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BENDEA ET AL

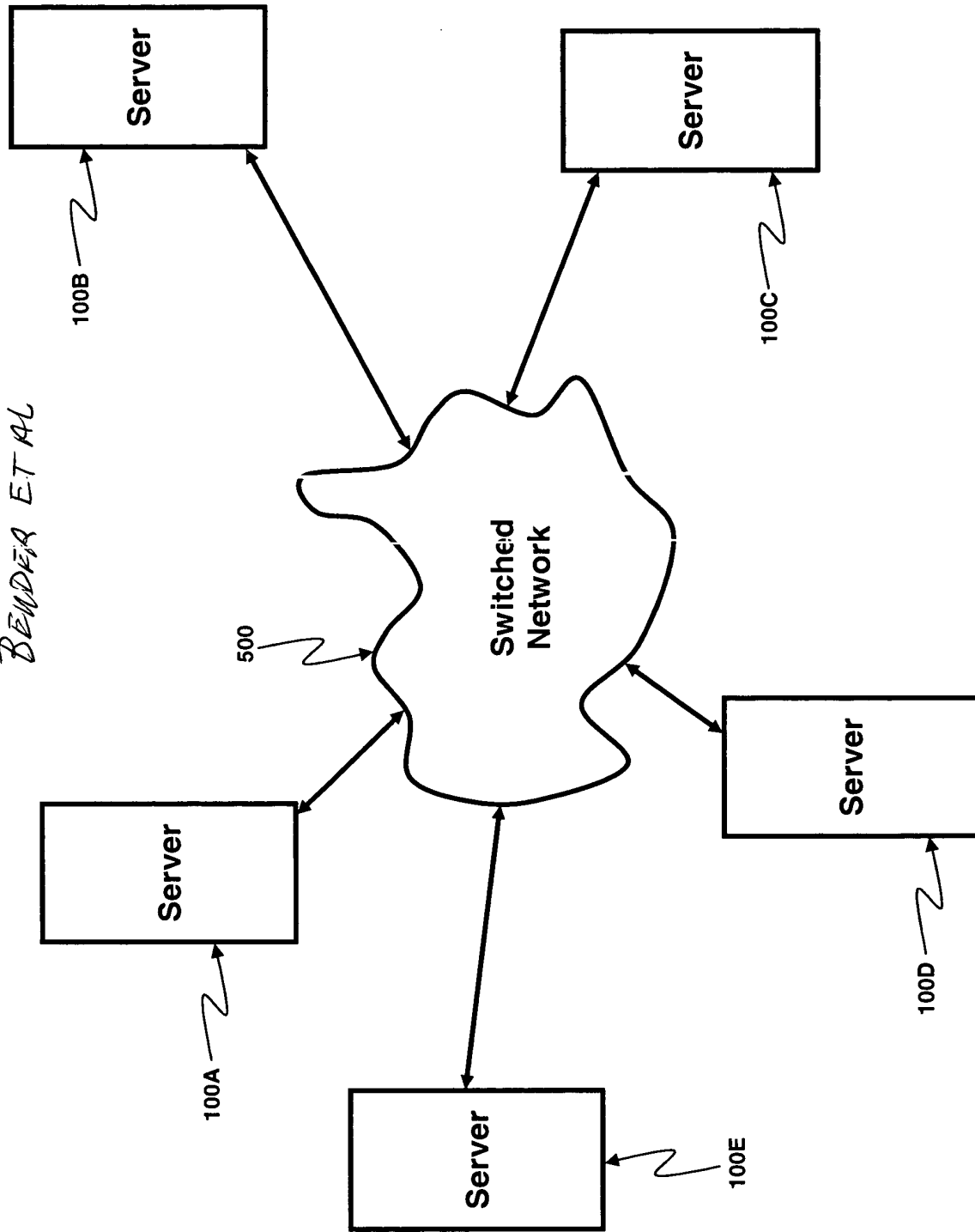


Figure 1

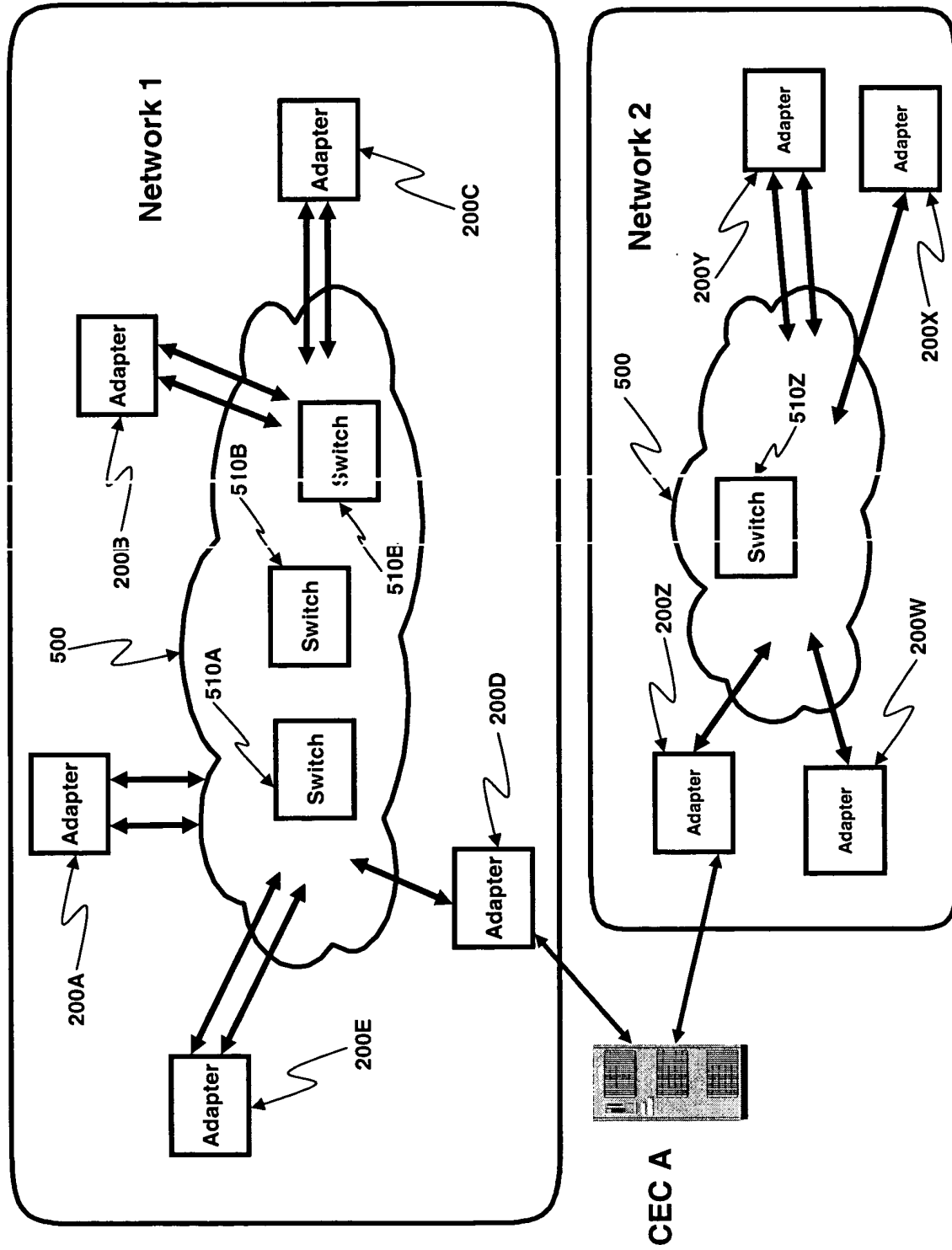


Figure 2

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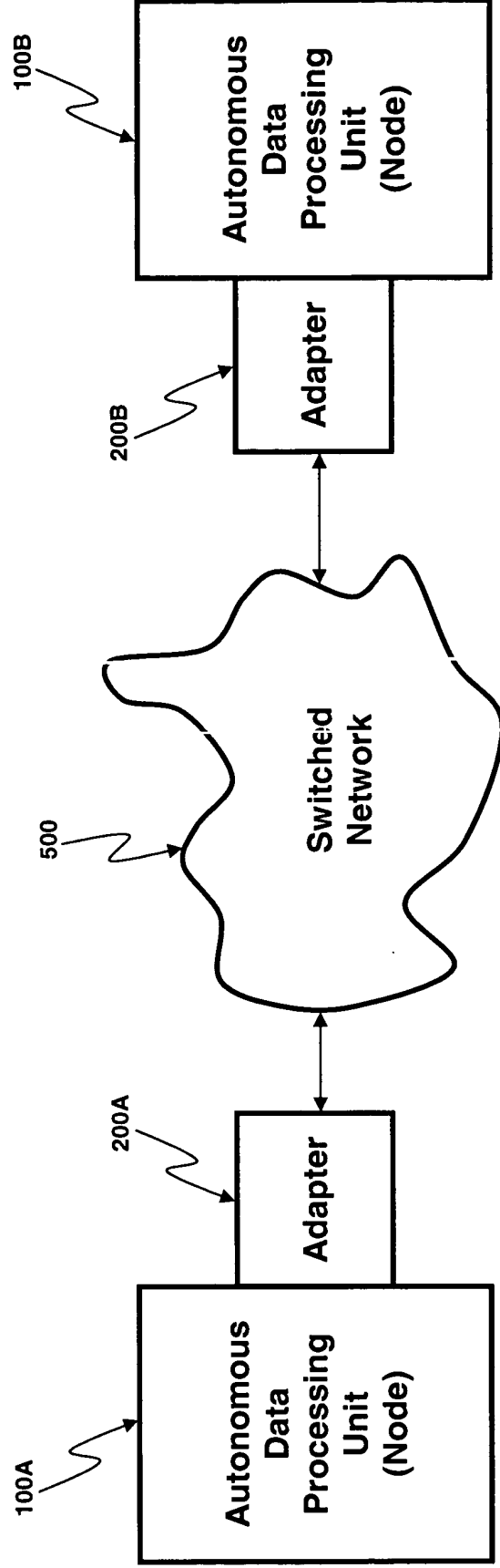


Figure 3

Send-Receive

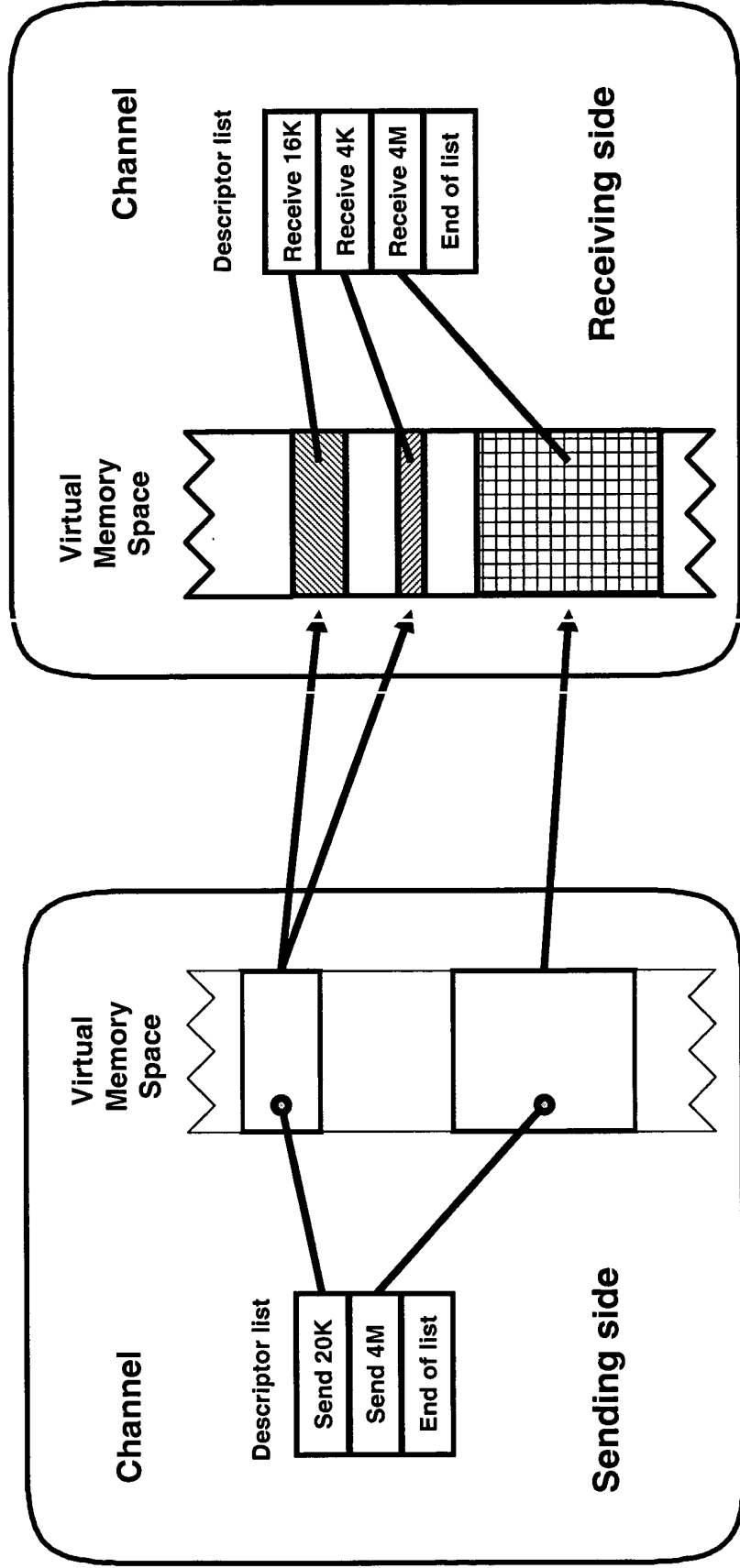


Figure 4

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Remote Read-Write

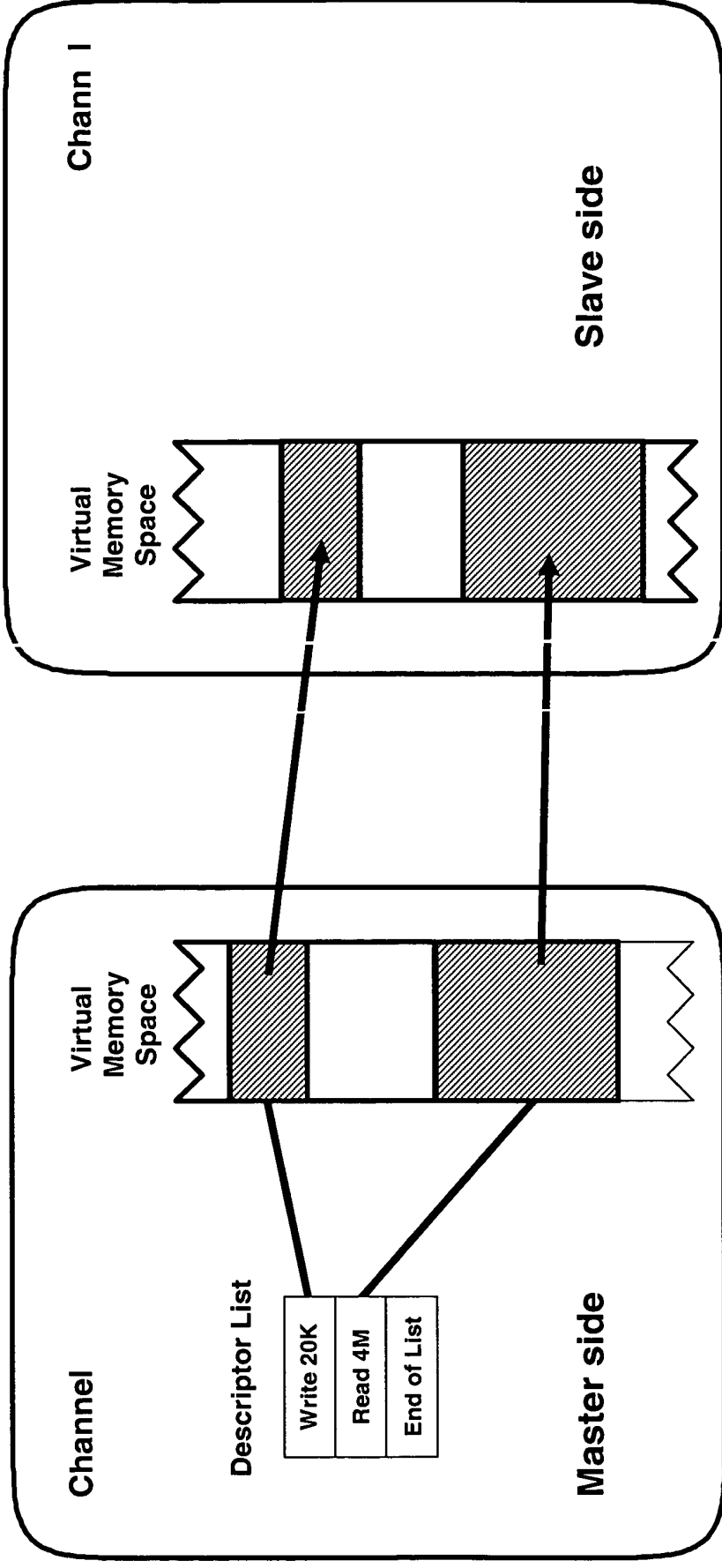


Figure 5

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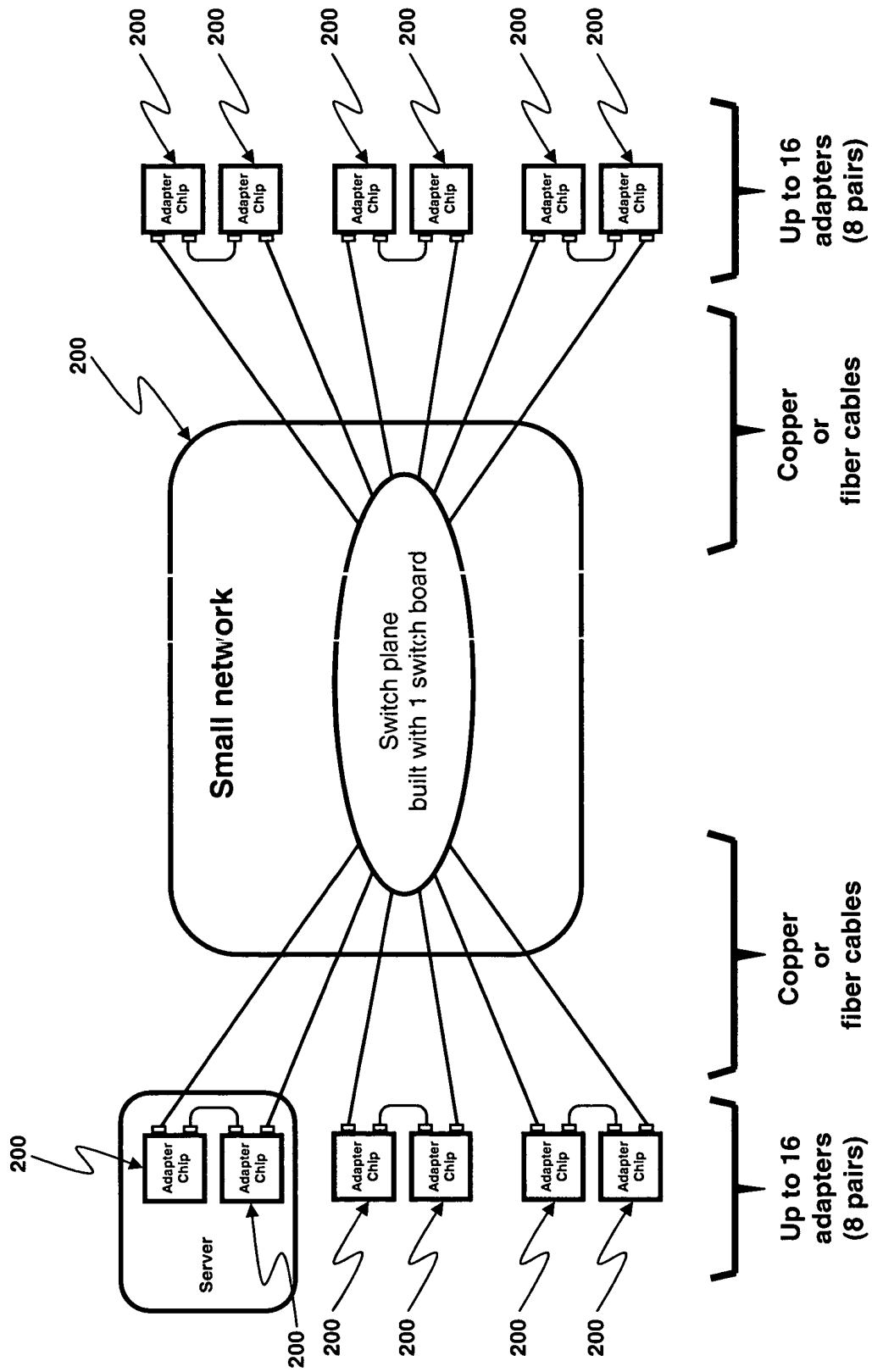


Figure 6

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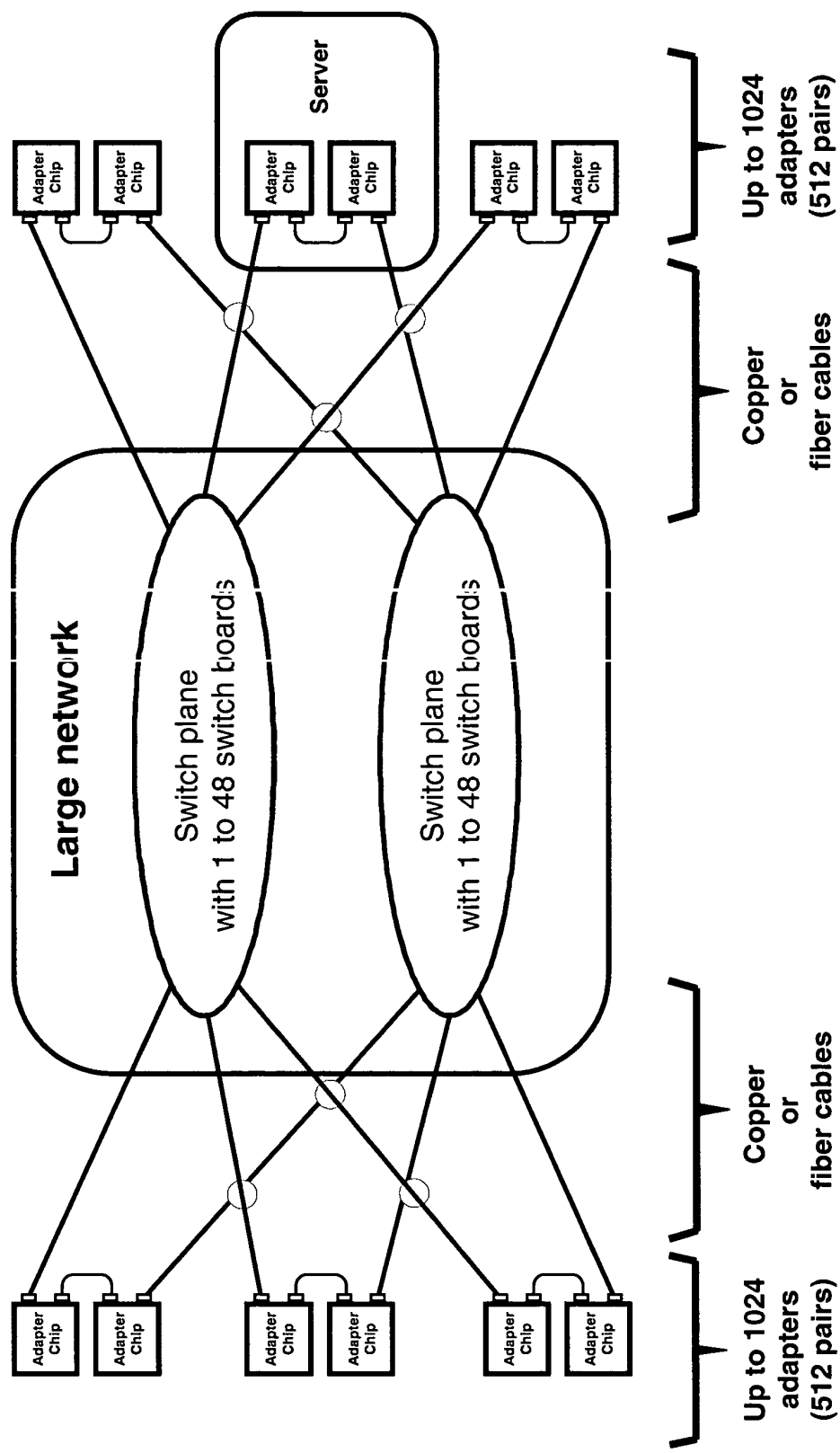


Figure 7

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Programming Interface

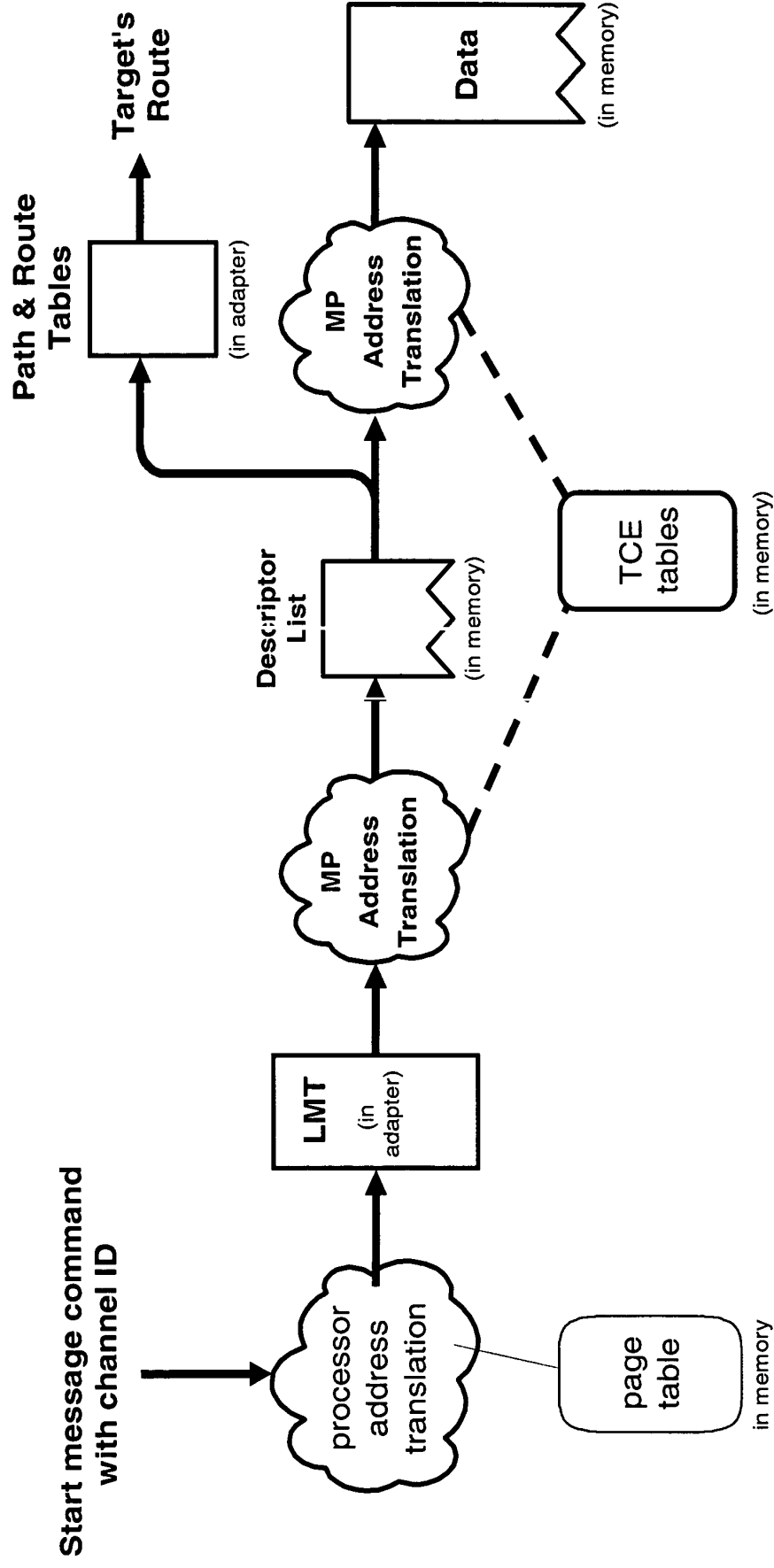


Figure 8

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Address Translation

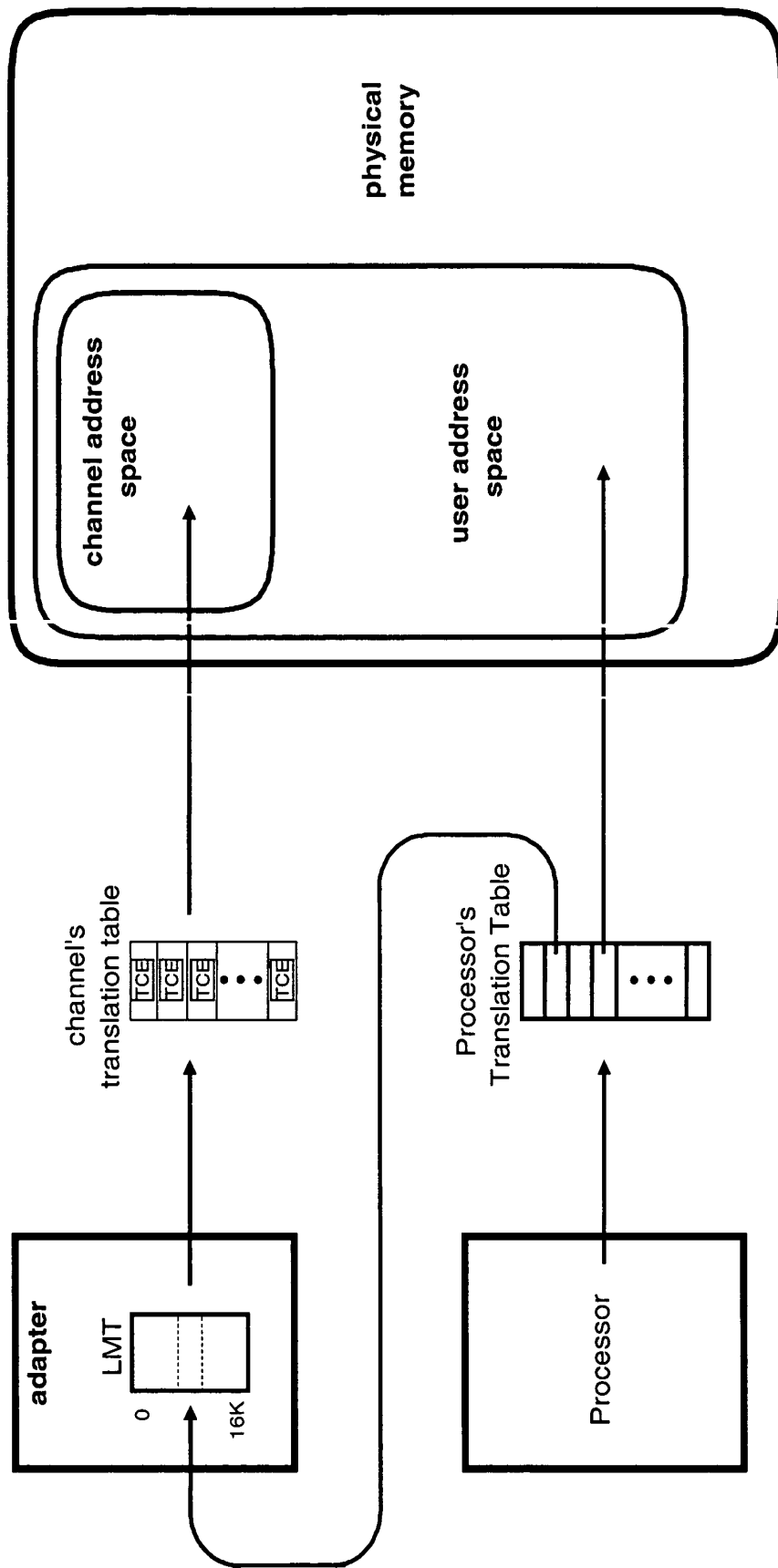


Figure 9

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Address Translation with 4K pages

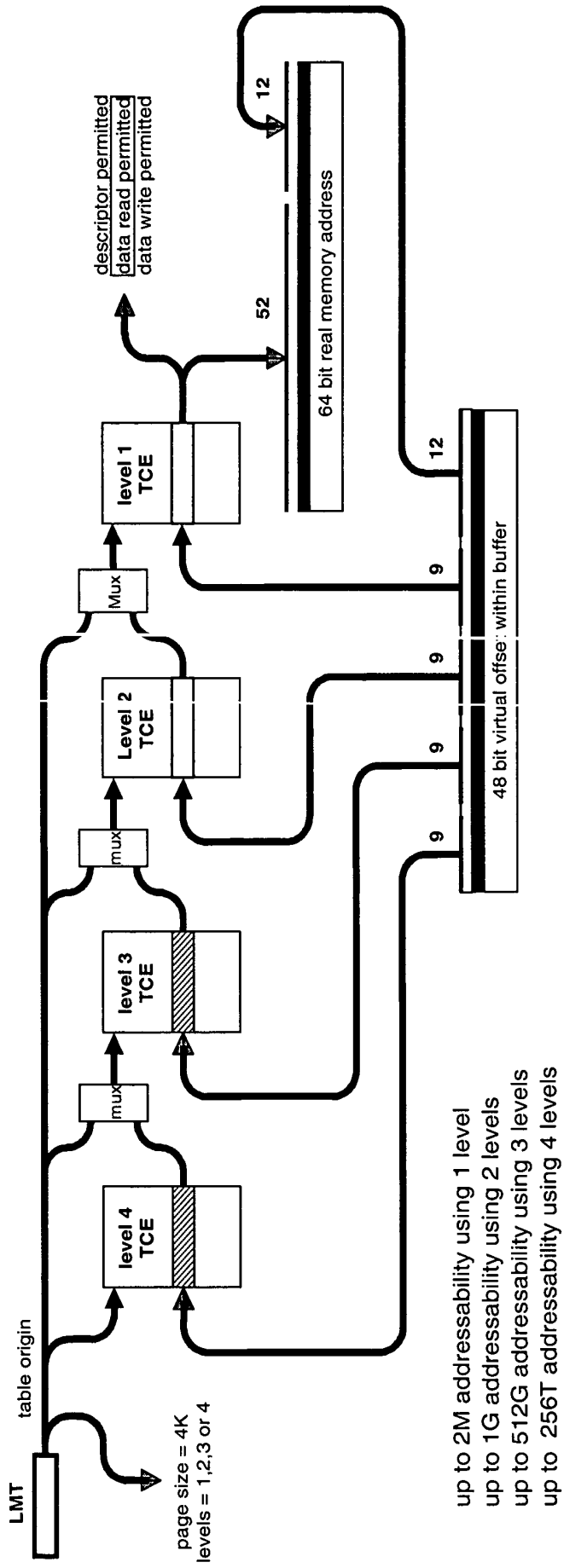


Figure 10

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Address Translation with 16M pages

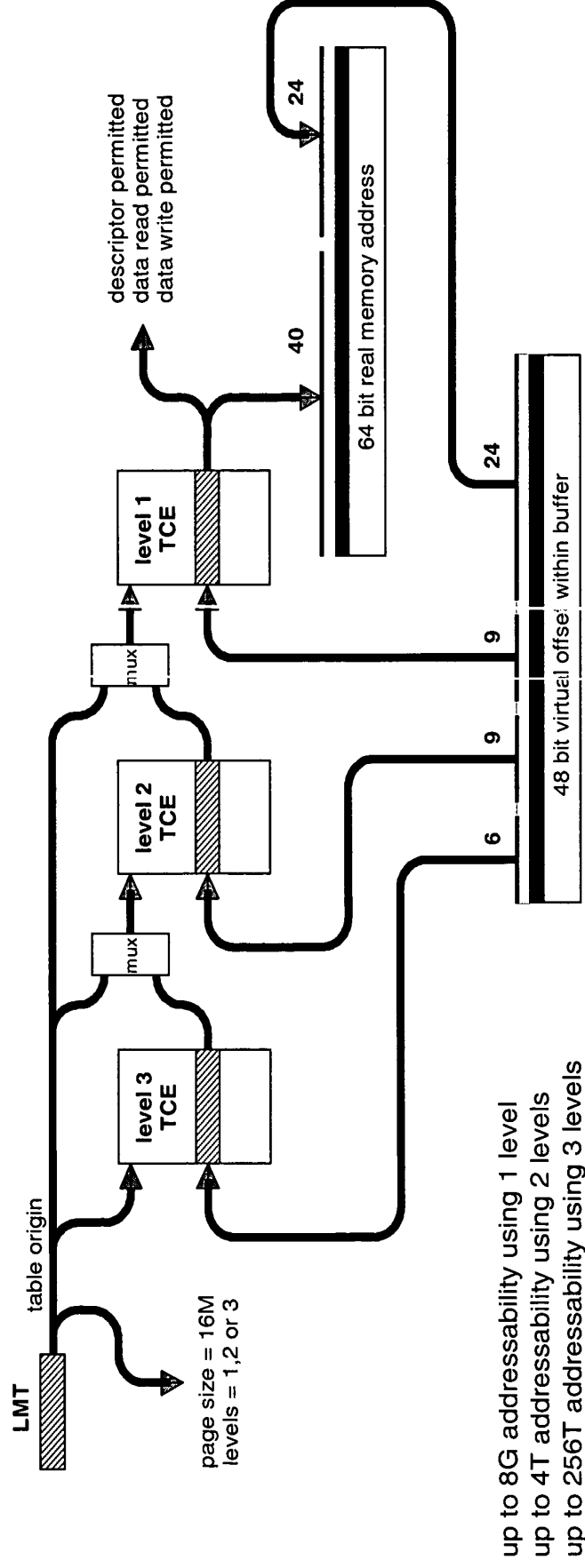


Figure 11

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Adapter Identification

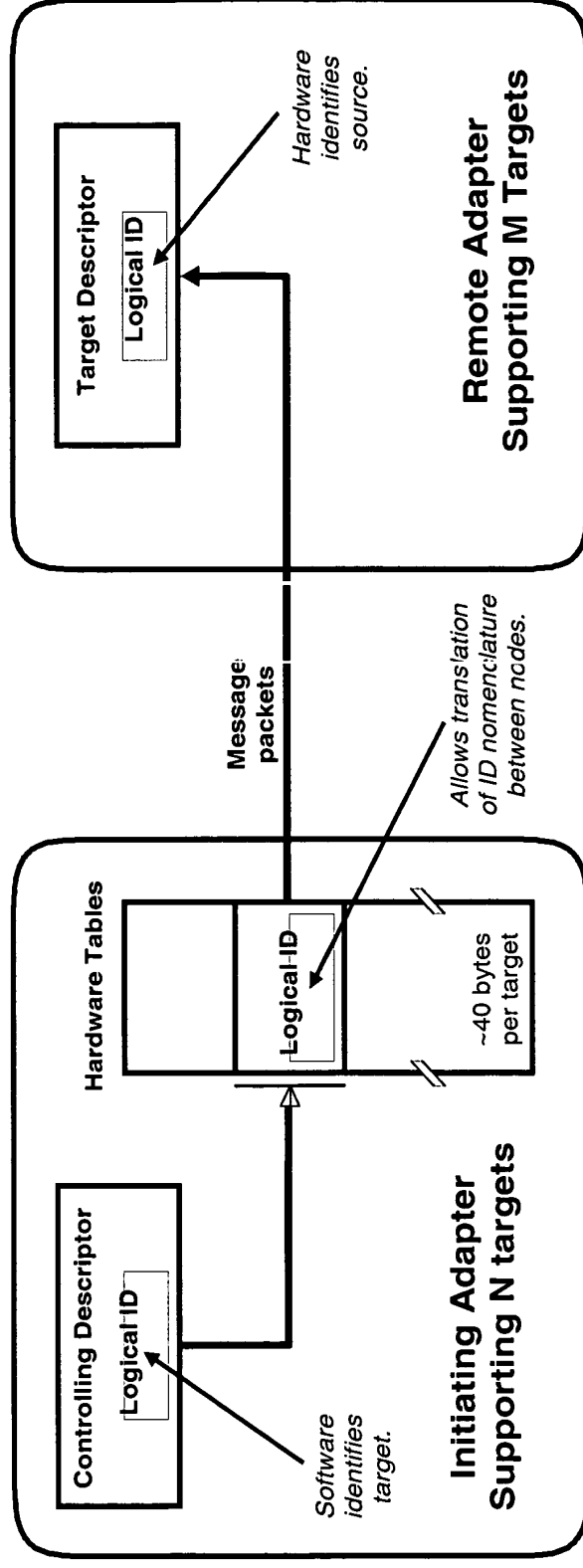


Figure 12

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Broadcast Function

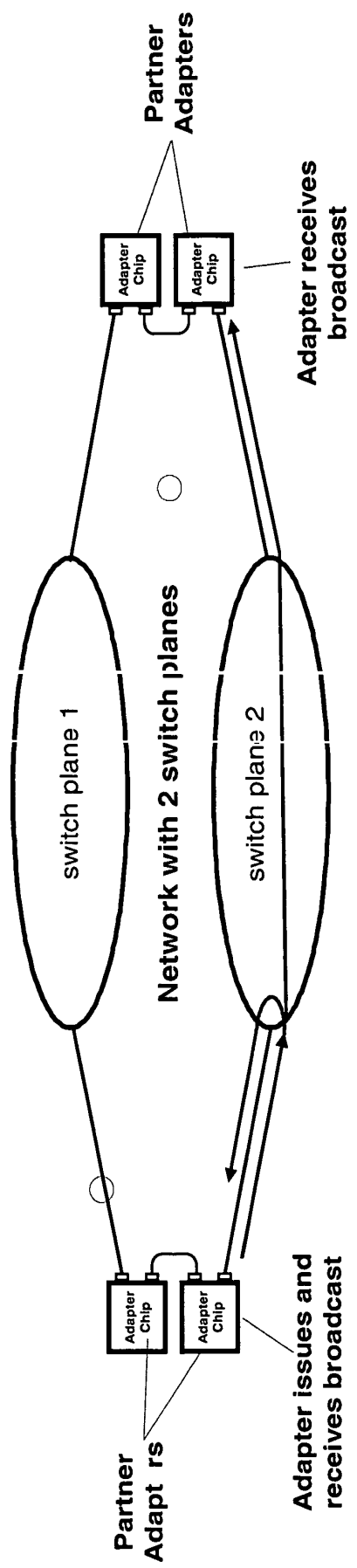


Figure 13

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Processor Interrupts

Channel Interrupt Generation

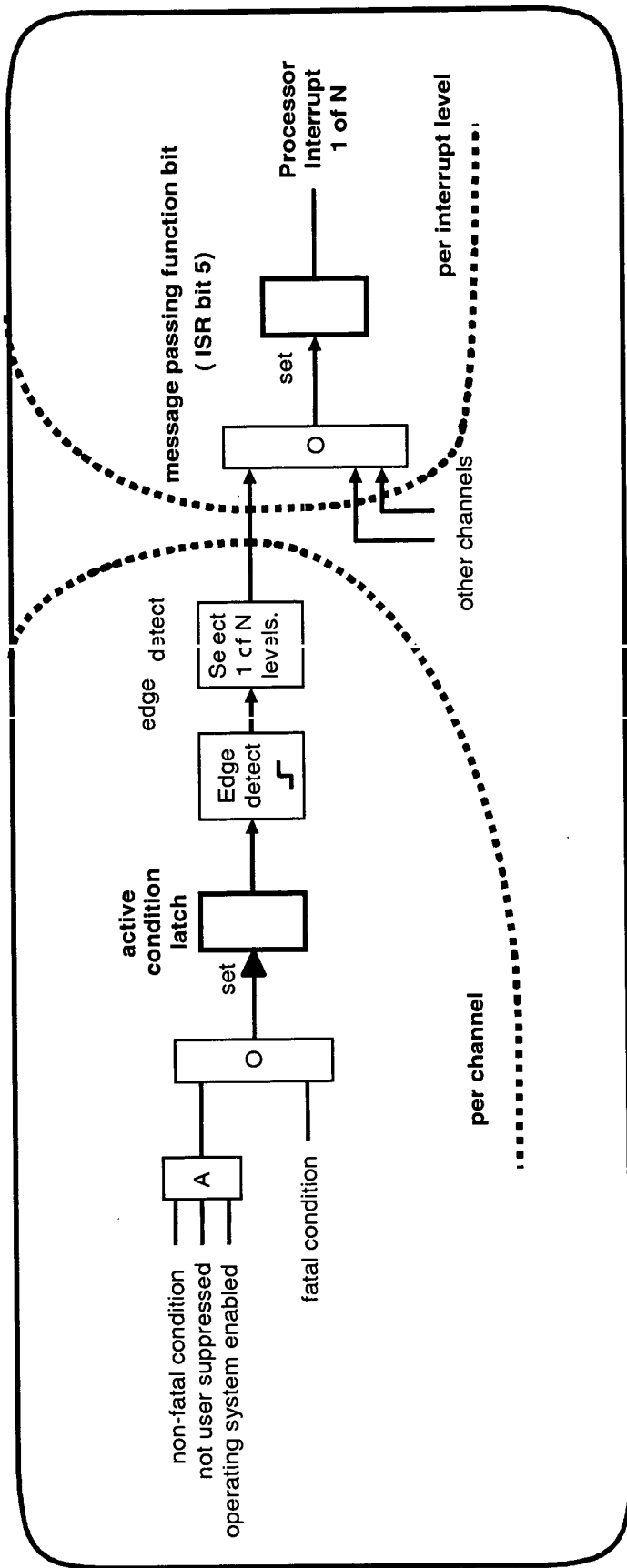


Figure 14

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Defined Address Fields

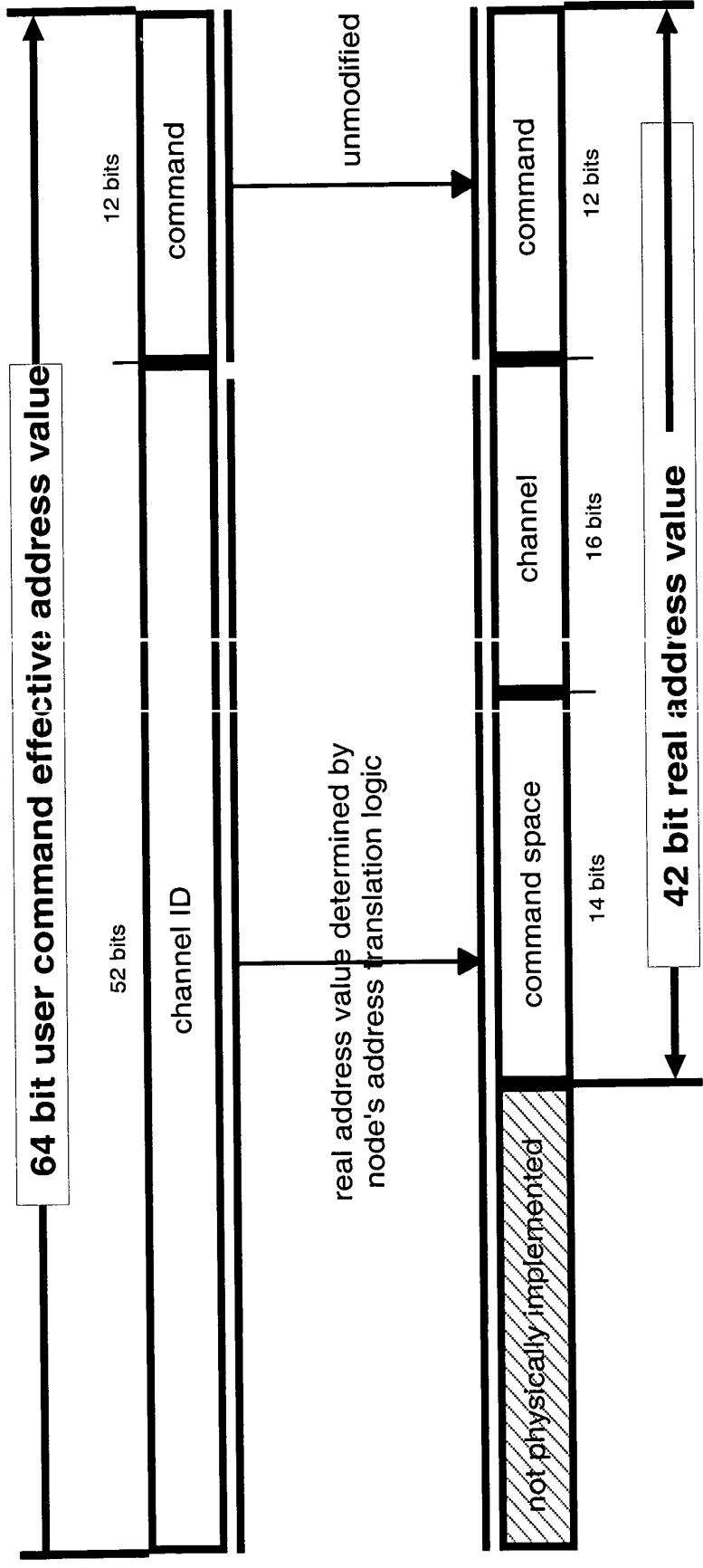


Figure 15

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Channel States

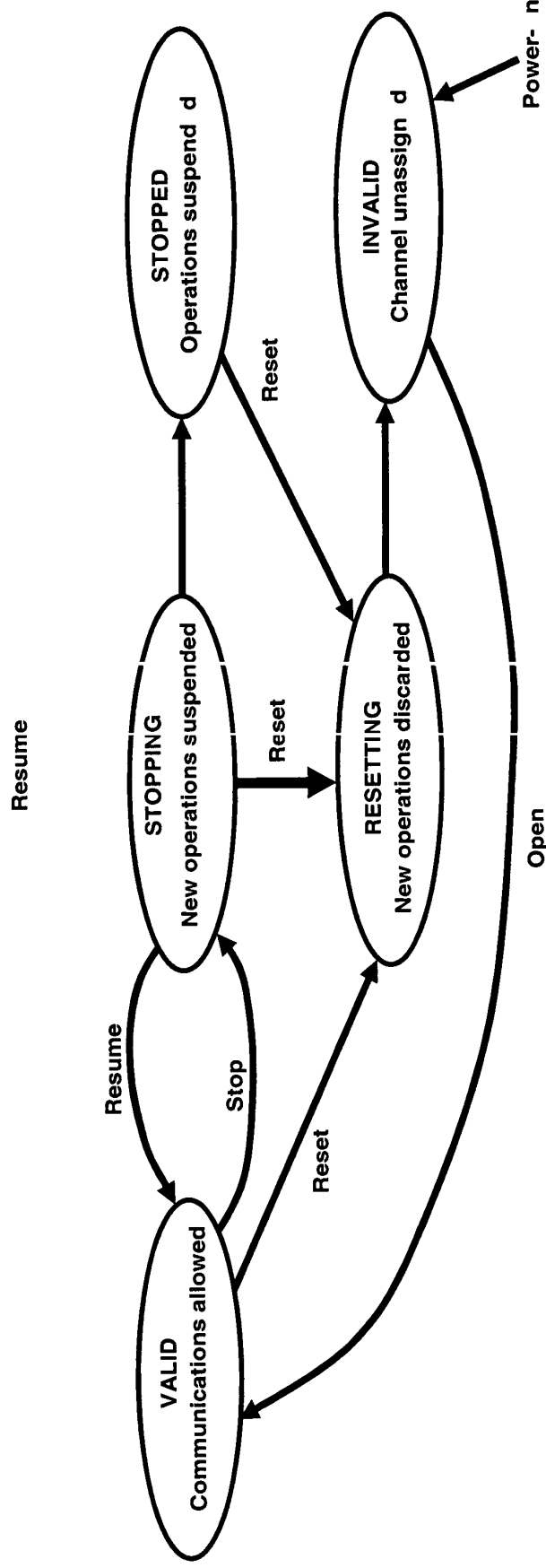


Figure 16

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Local Mapping Table (LMT) Entries

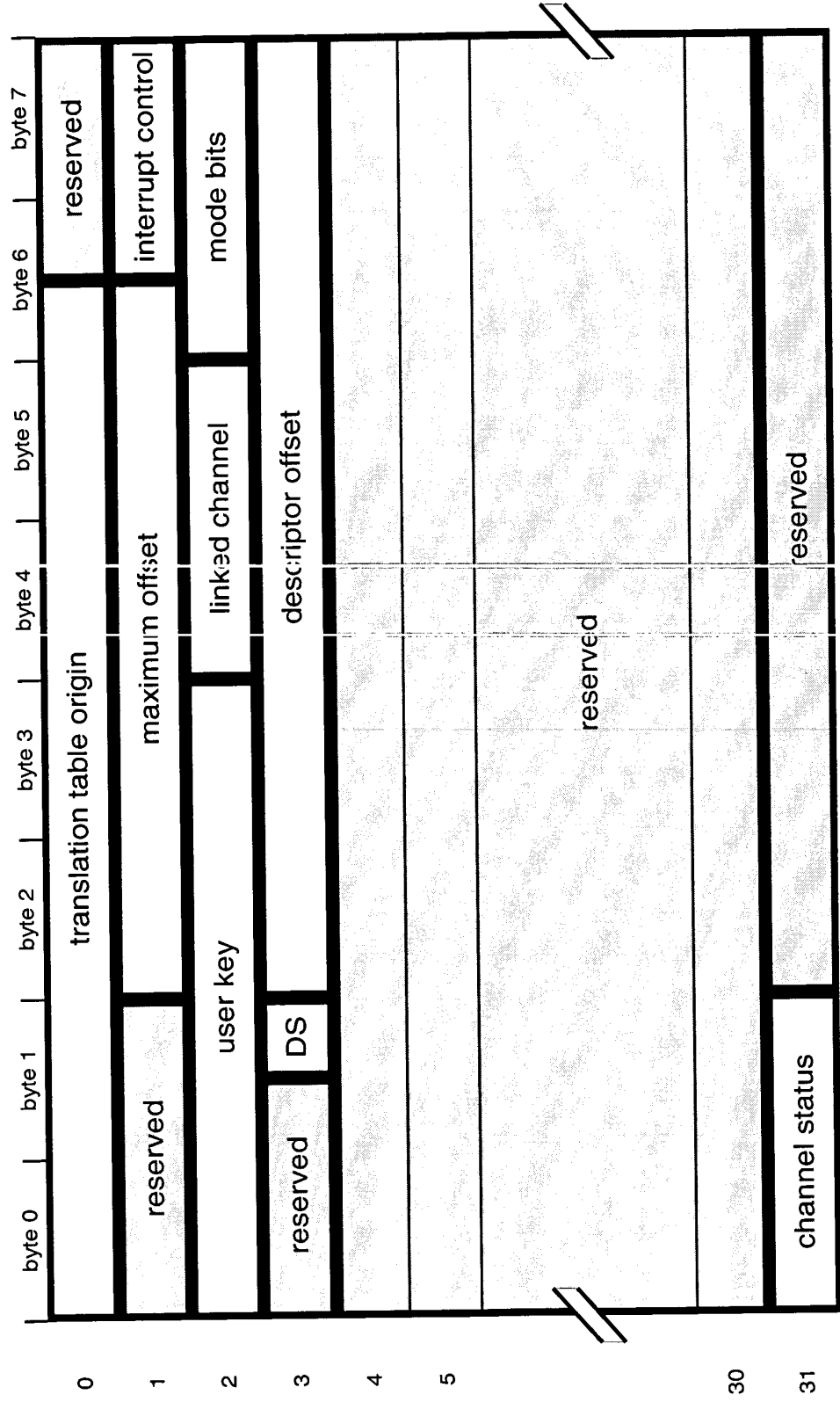


Figure 17

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Translation Control Elements

TCE format

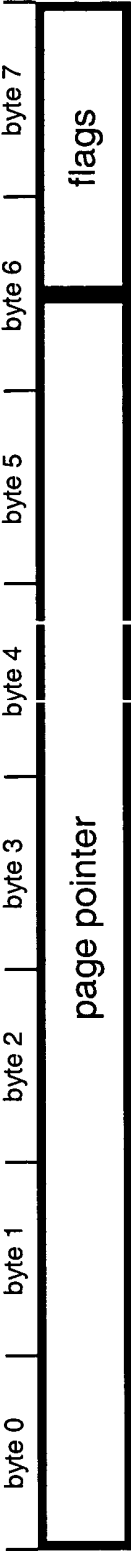


Figure 18

Remote Write

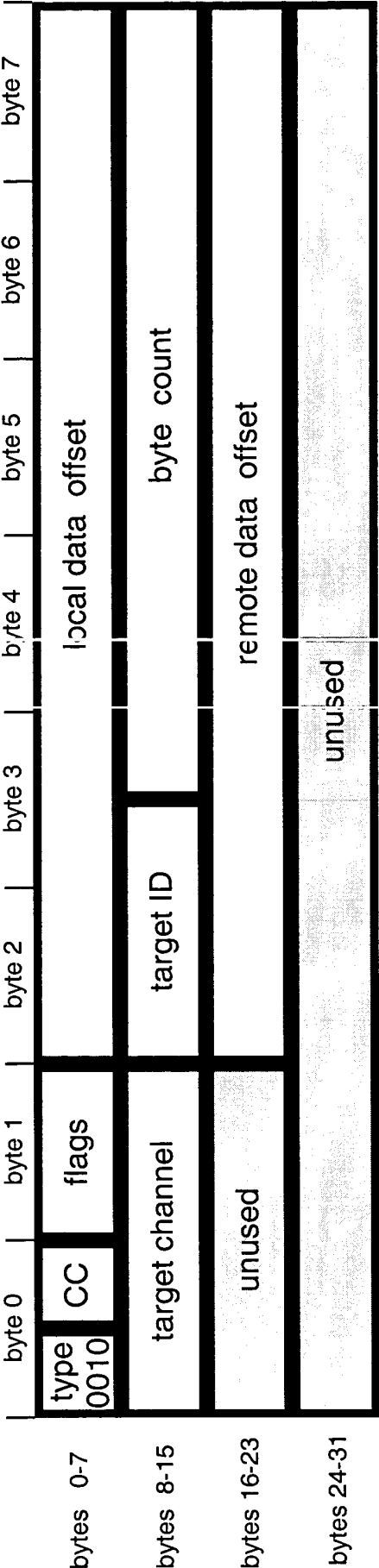


Figure 19

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Remote Read

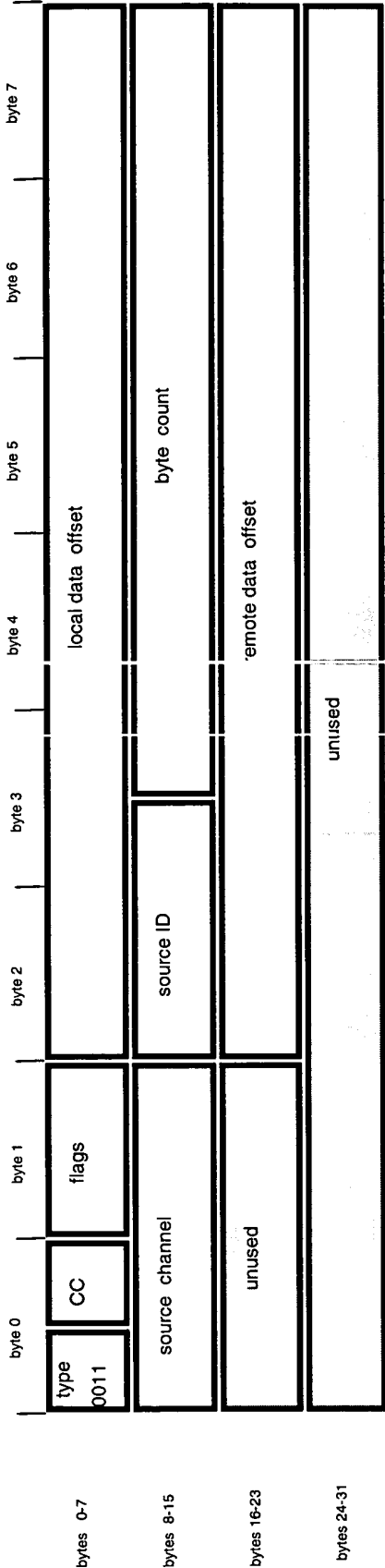


Figure 20

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Source of Push

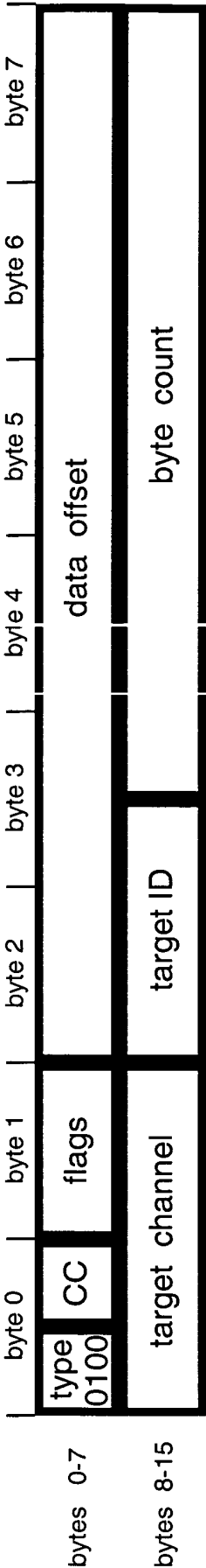


Figure 21

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Target of push

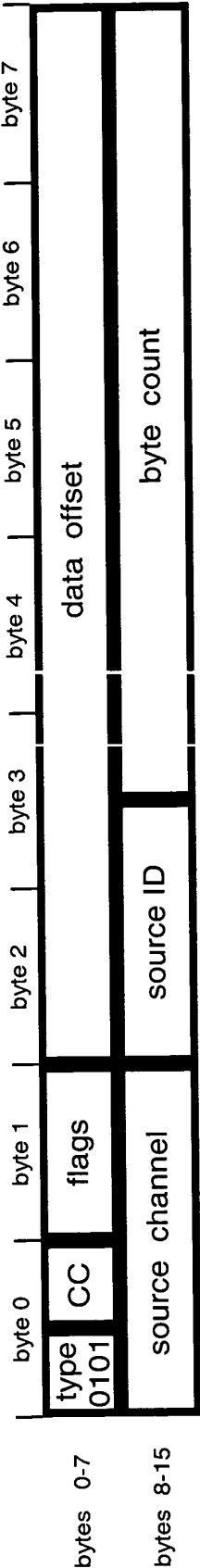


Figure 22

Source of Pull

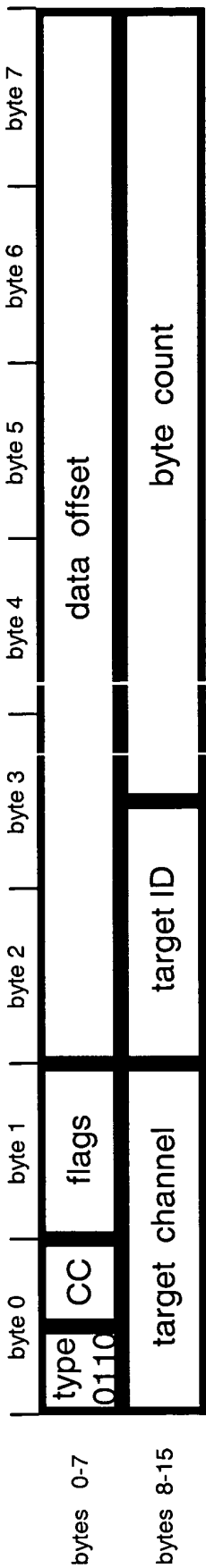


Figure 23

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Target of pull

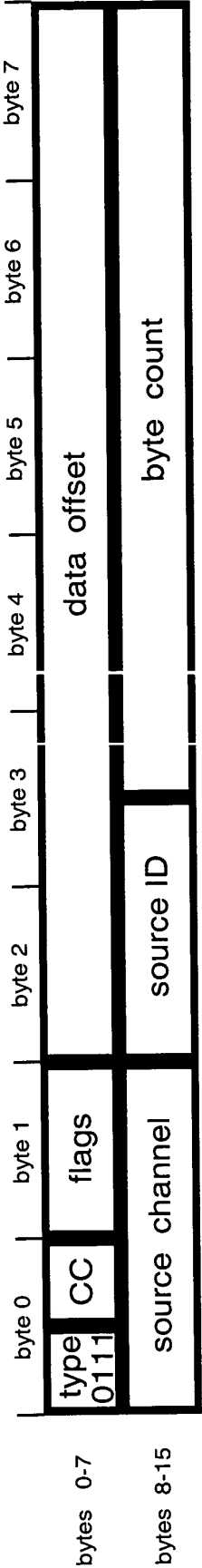


Figure 24

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Preload data

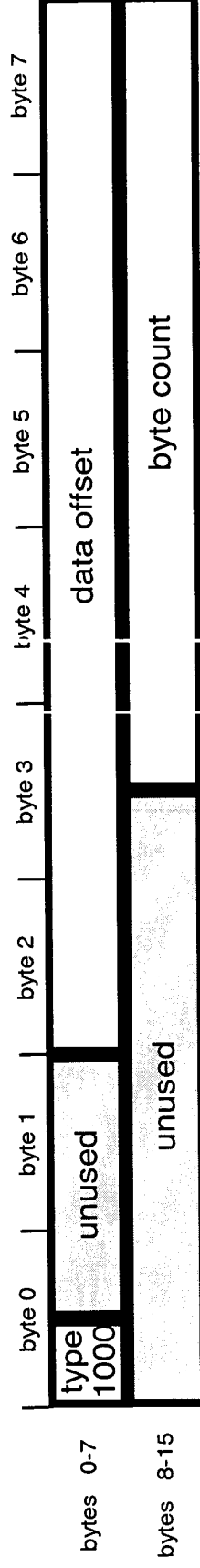


Figure 25

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Branch

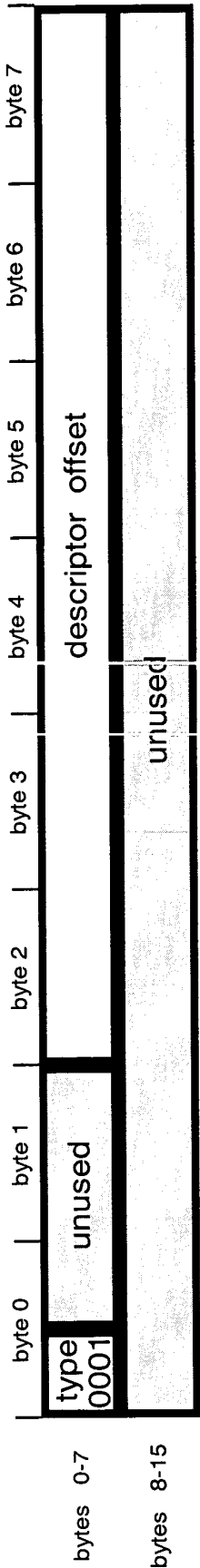


Figure 26

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Path Table Entry



Figure 27

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Route Table Entry

	byte 0	byte 1	byte 2	byte 3	byte 4	byte 5	byte 6	byte 7
path 0	0000	route nibbles						port
path 1	0000	route nibbles						port
path 2	0000	route nibbles						port
path 3	0000	route nibbles						port

Figure 28

Broadcast Registers

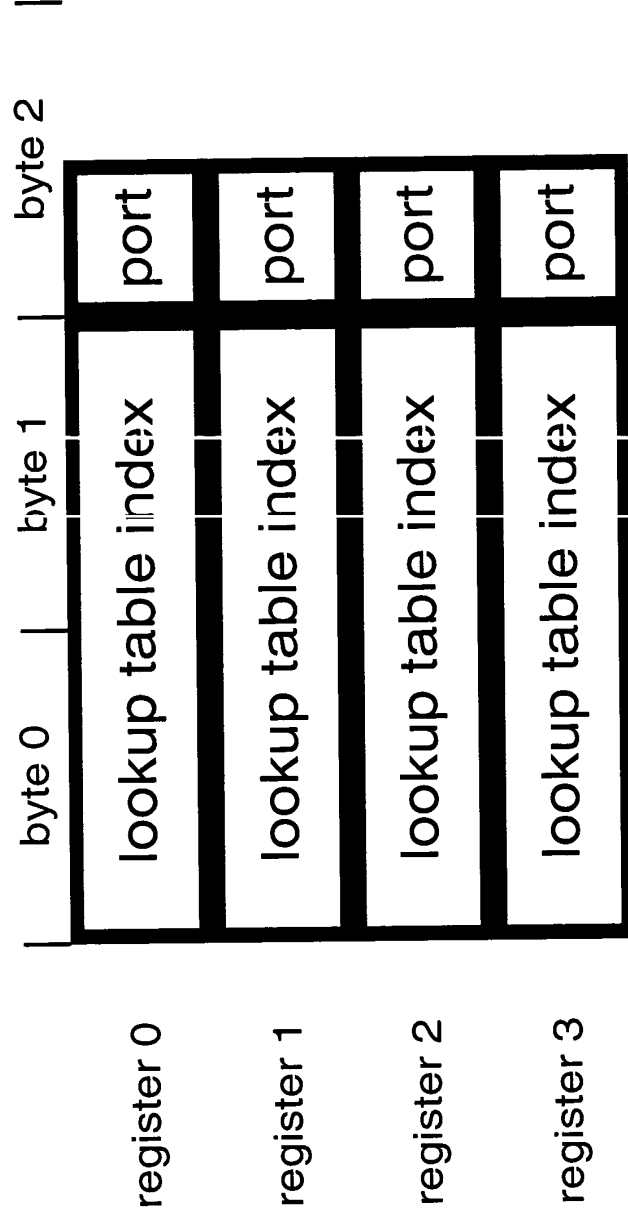


Figure 29

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Sequence Table Entry

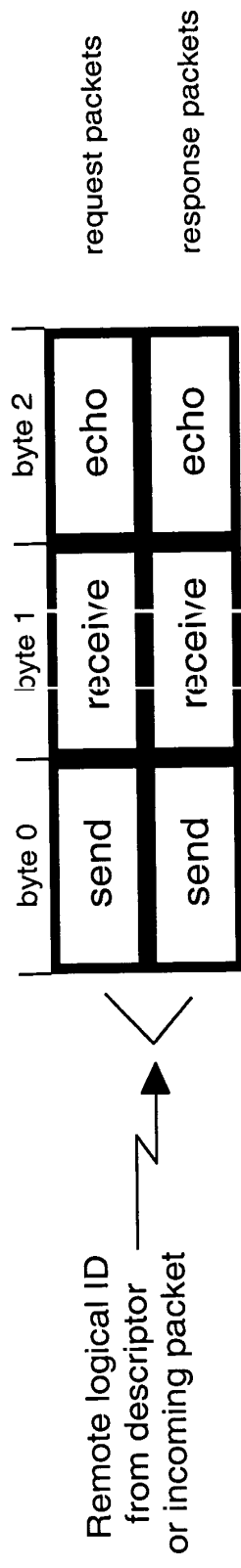


Figure 30

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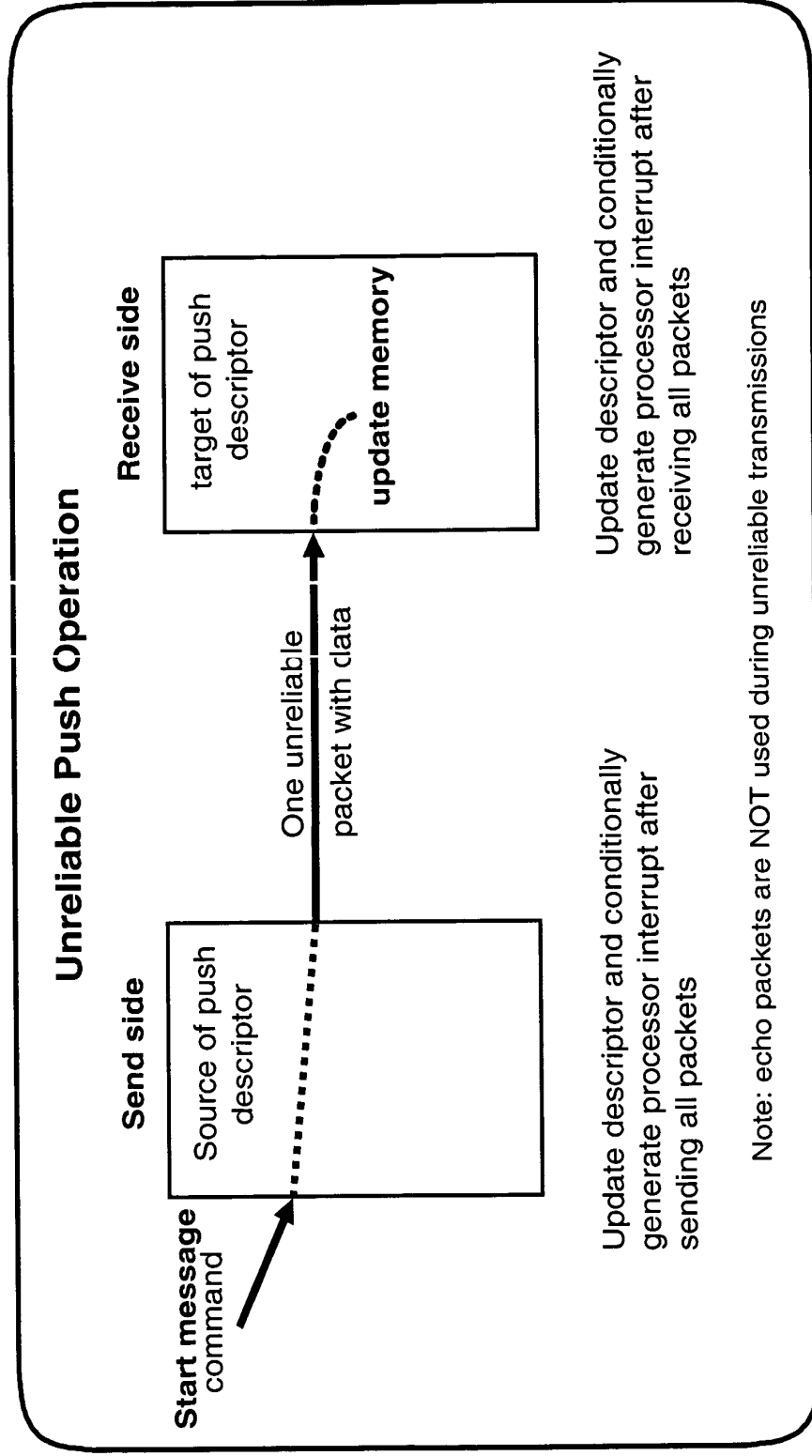


Figure 31

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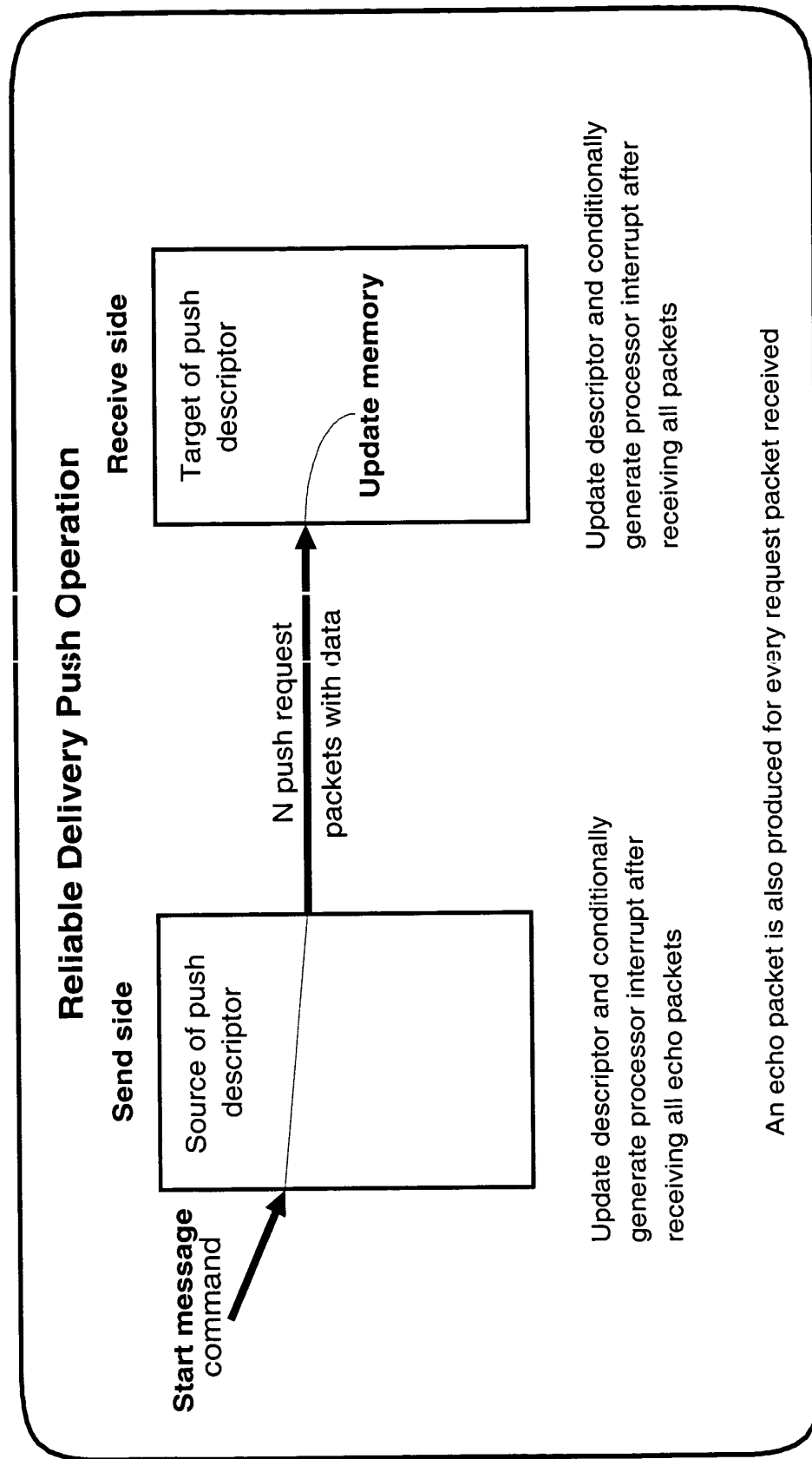


Figure 32

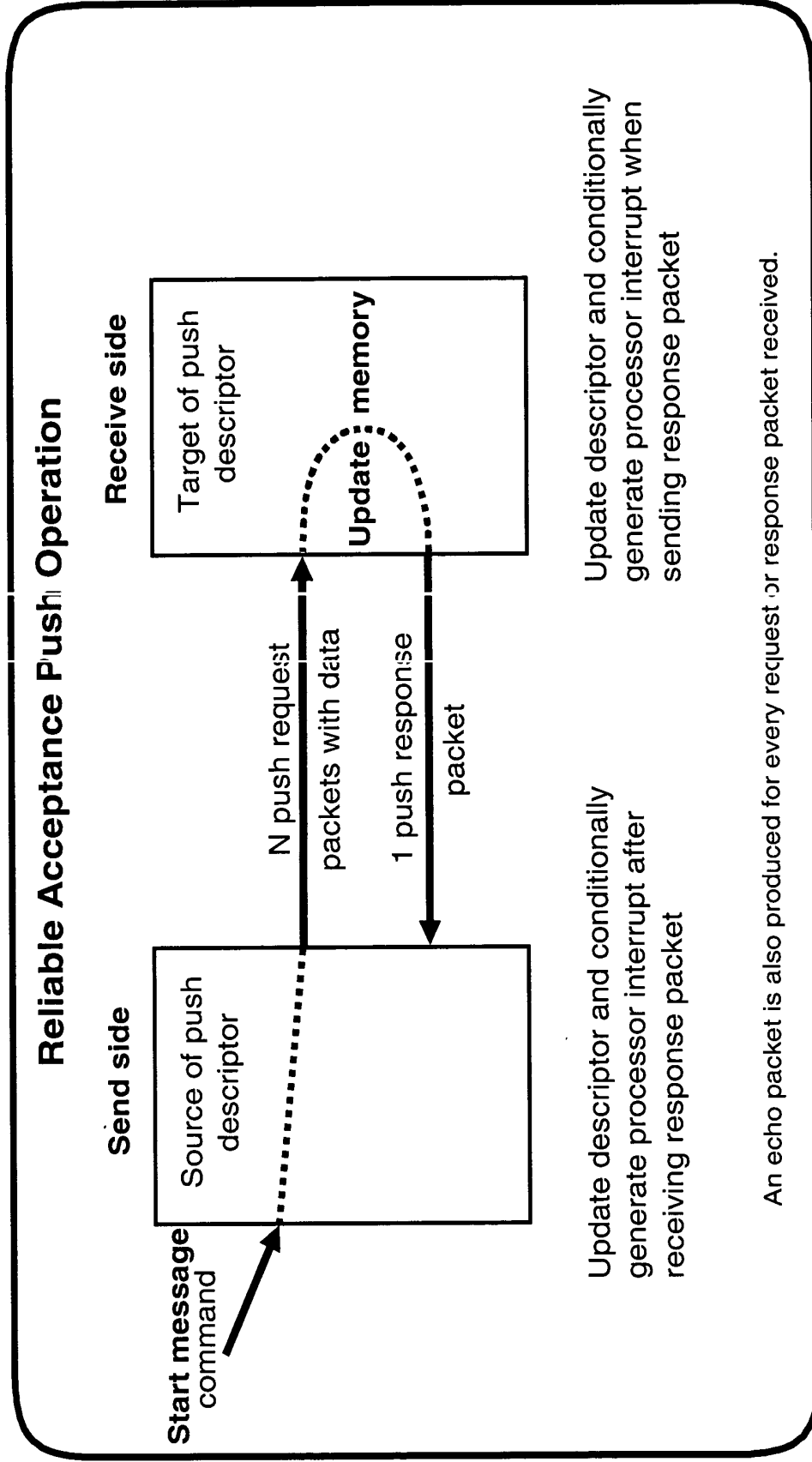


Figure 33

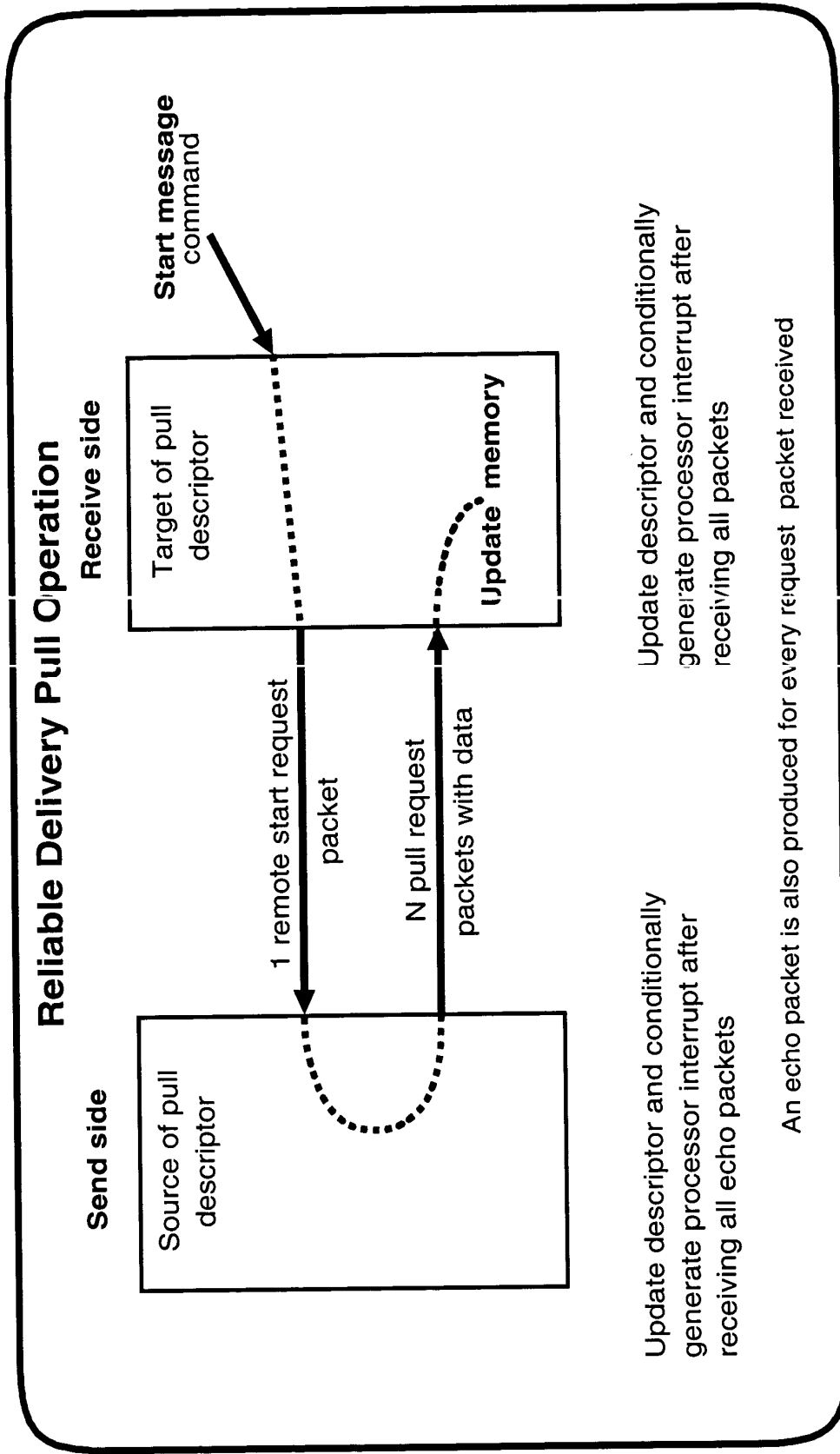


Figure 34

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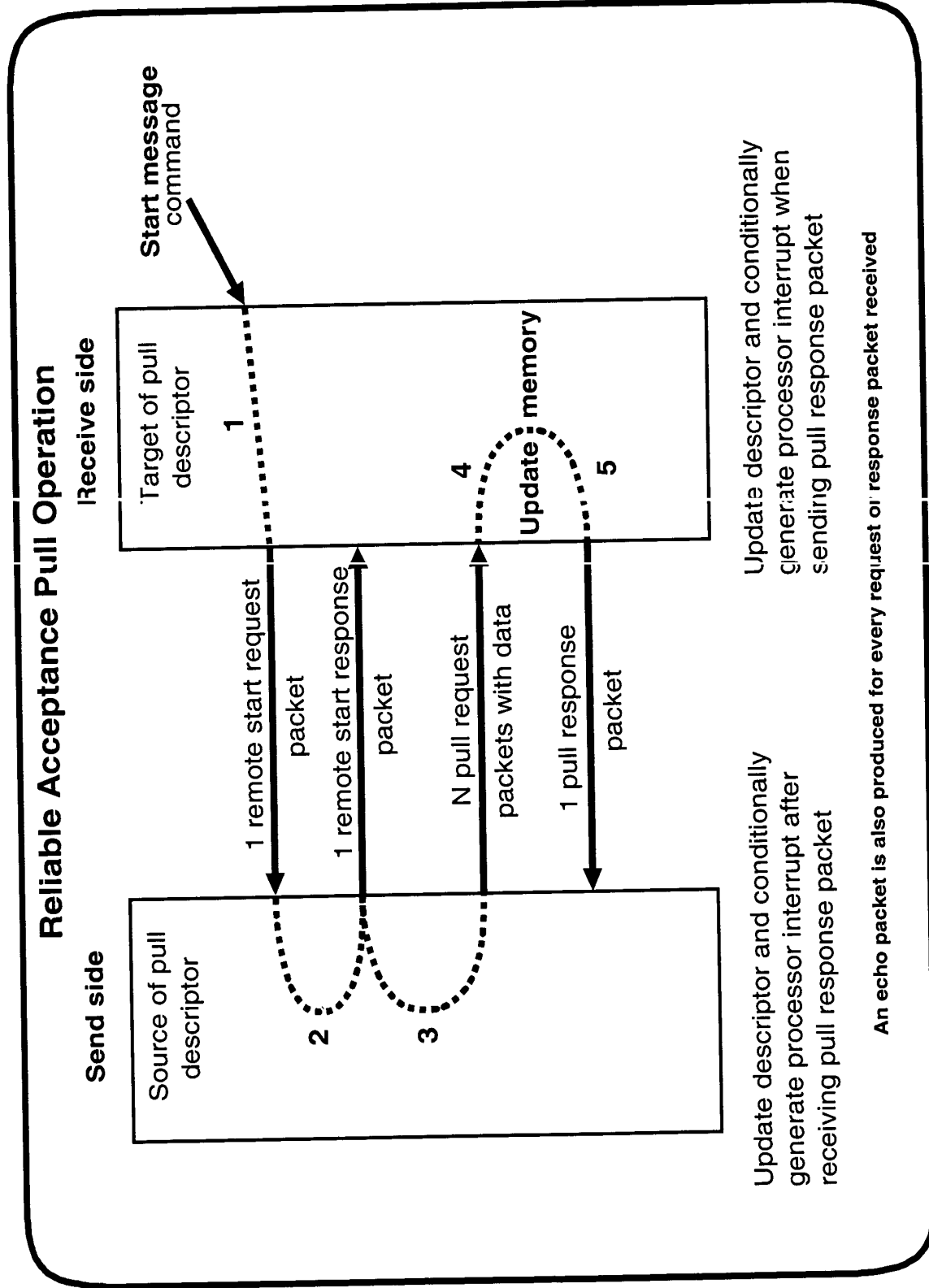


Figure 35

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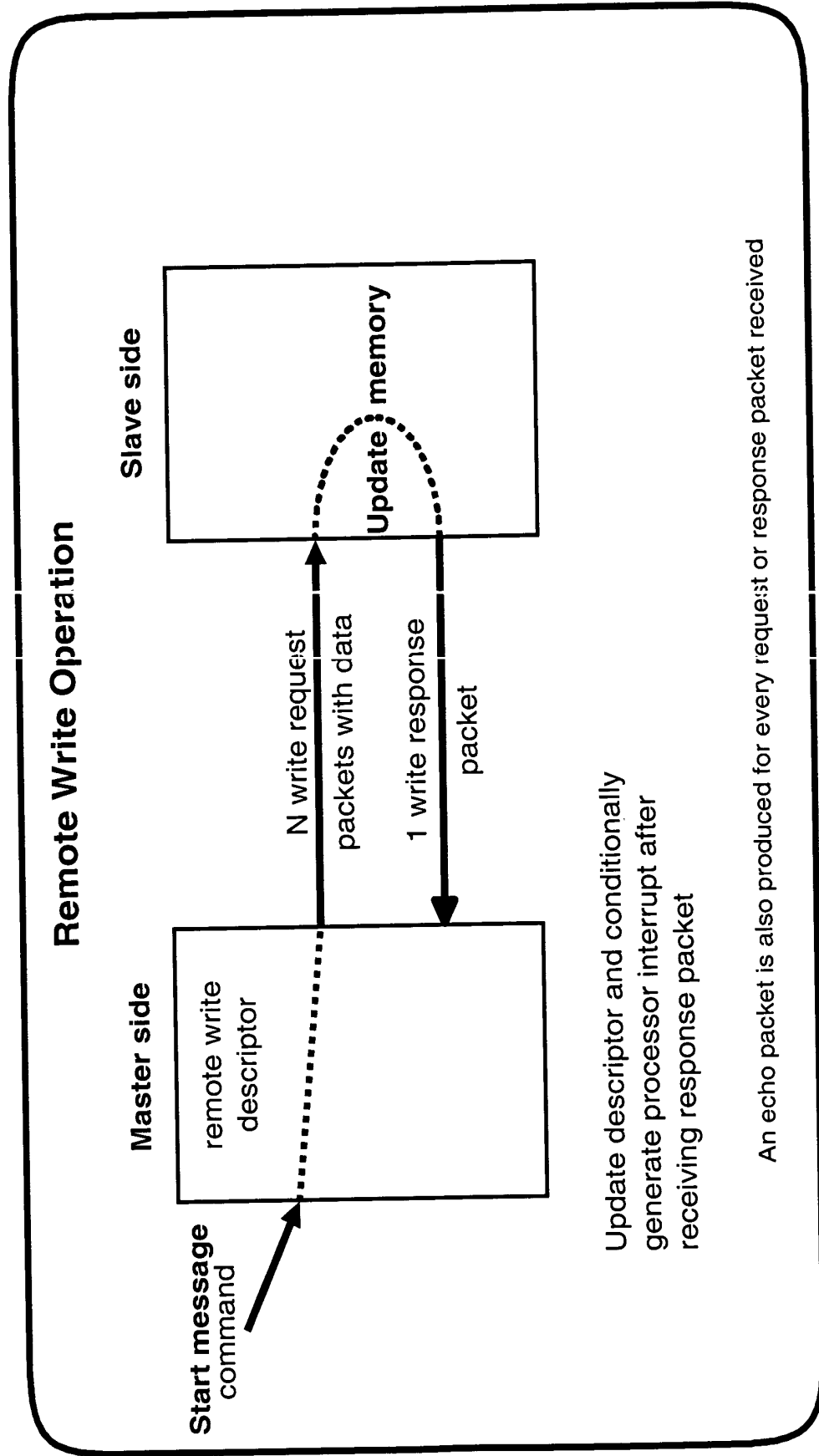
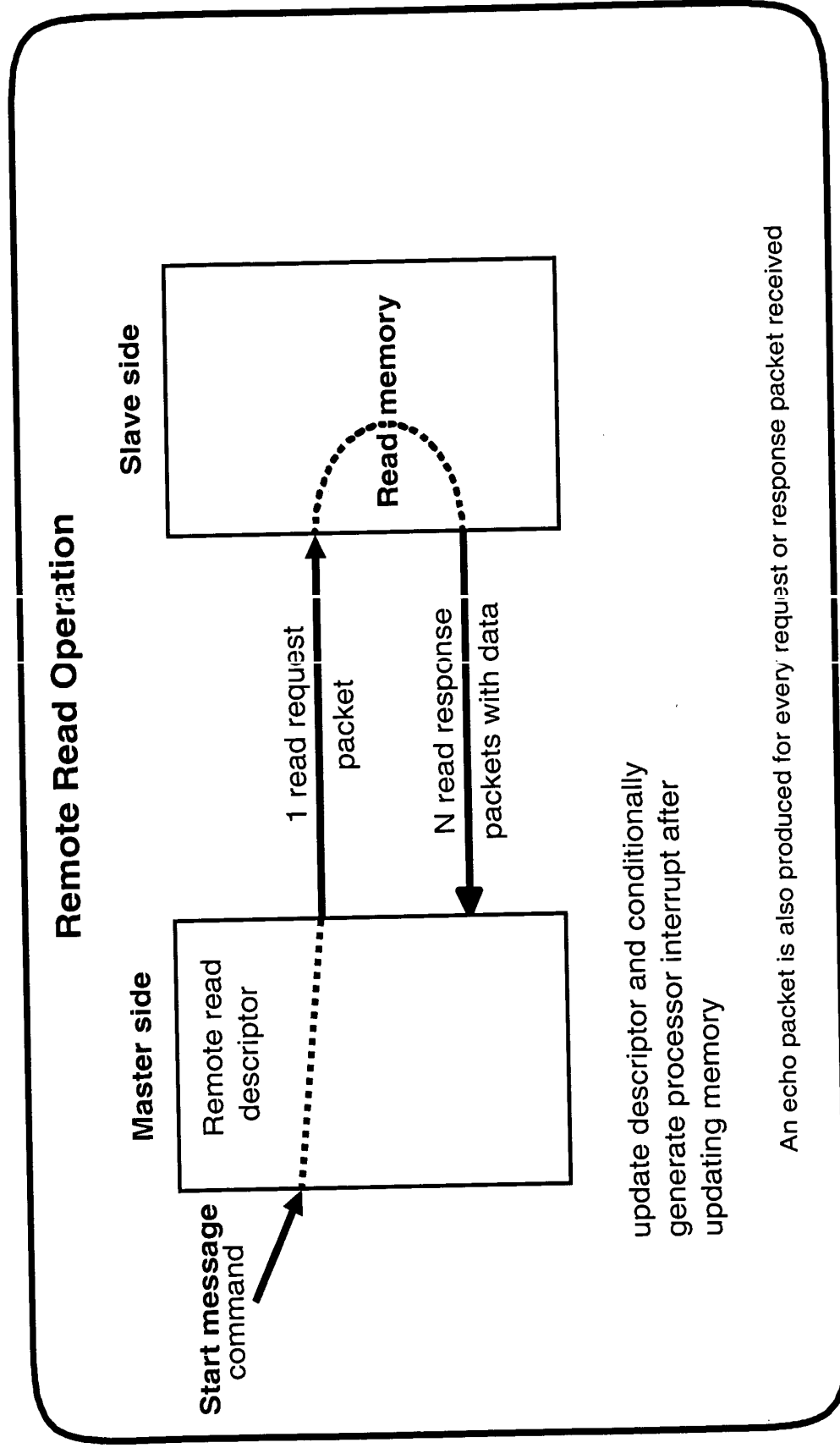
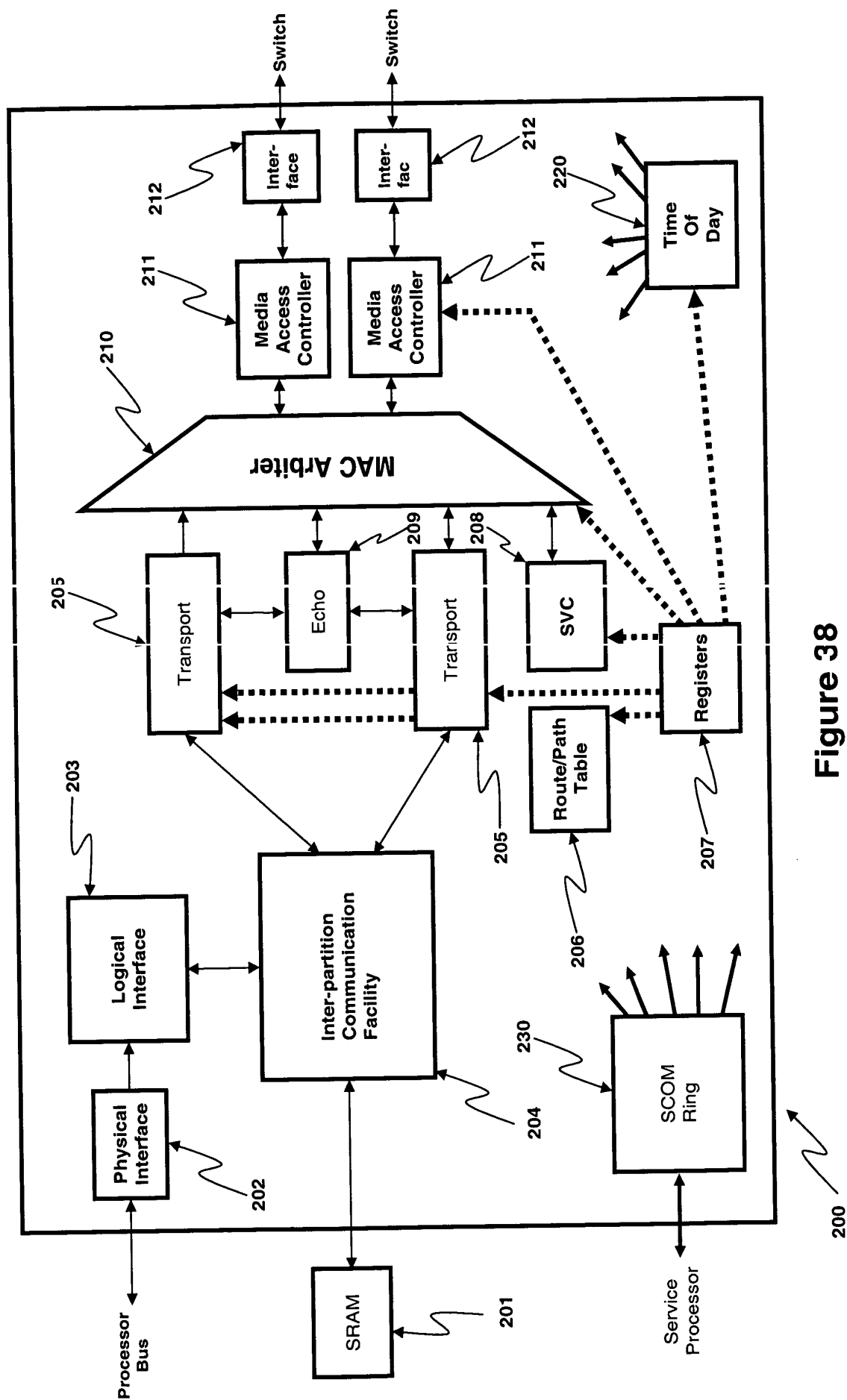


Figure 36

**Figure 37**

$$\frac{25}{3}$$


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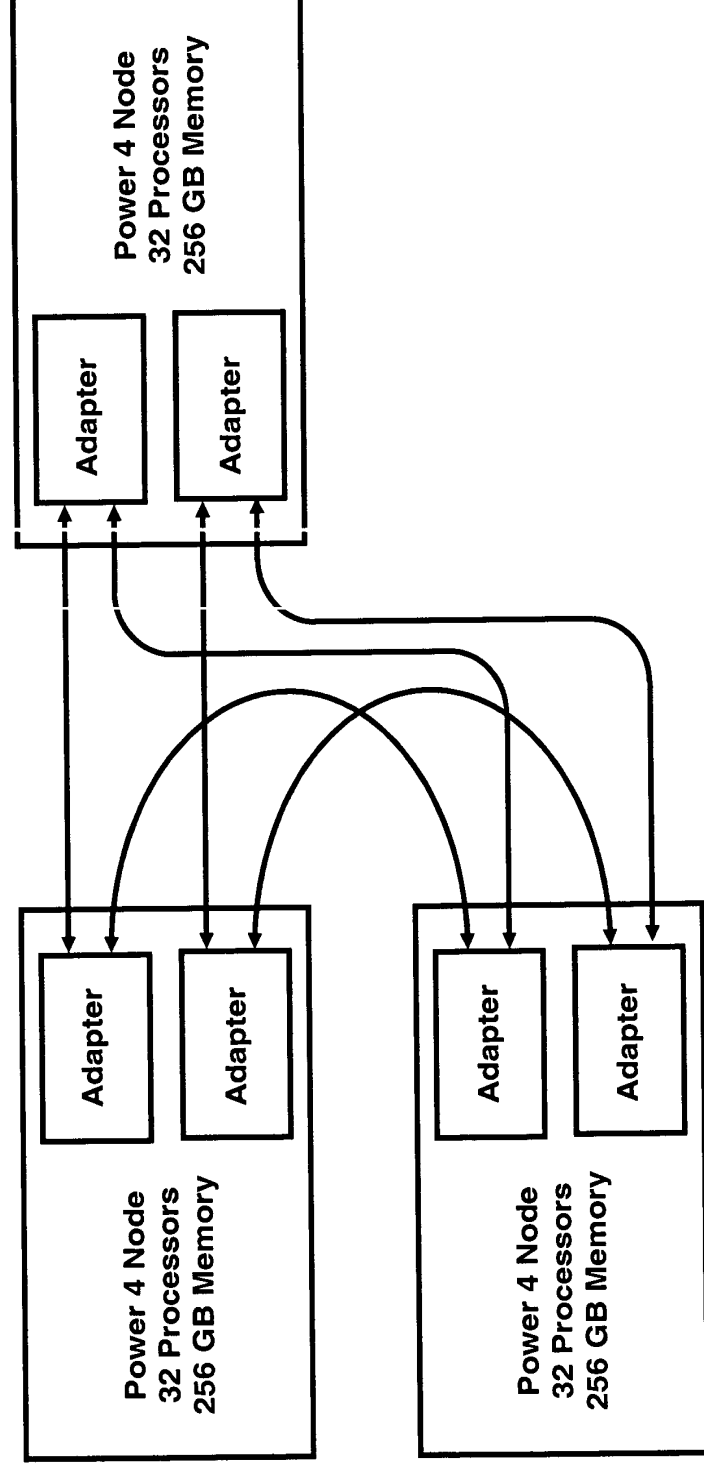


Figure 39

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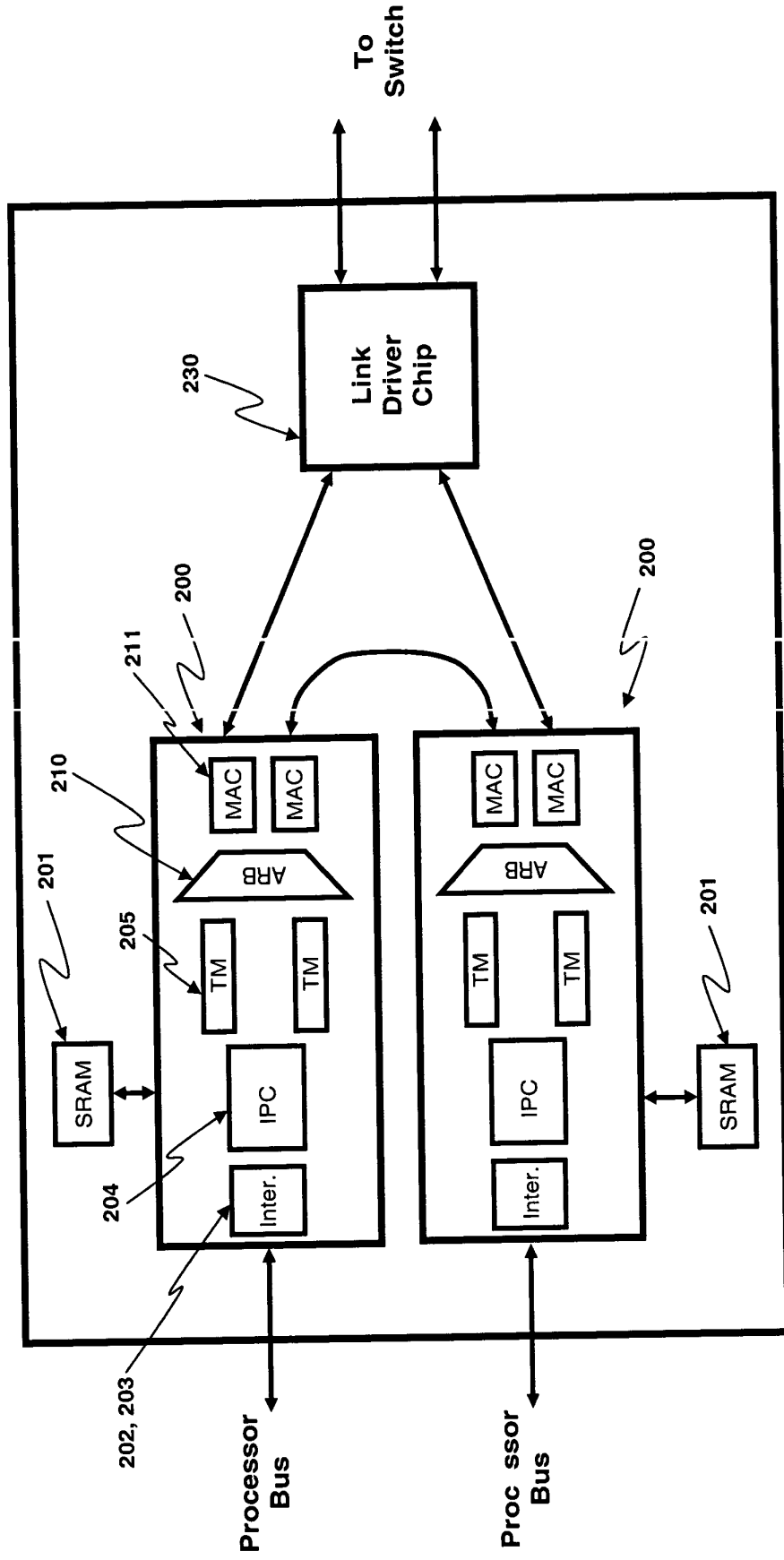


Figure 40

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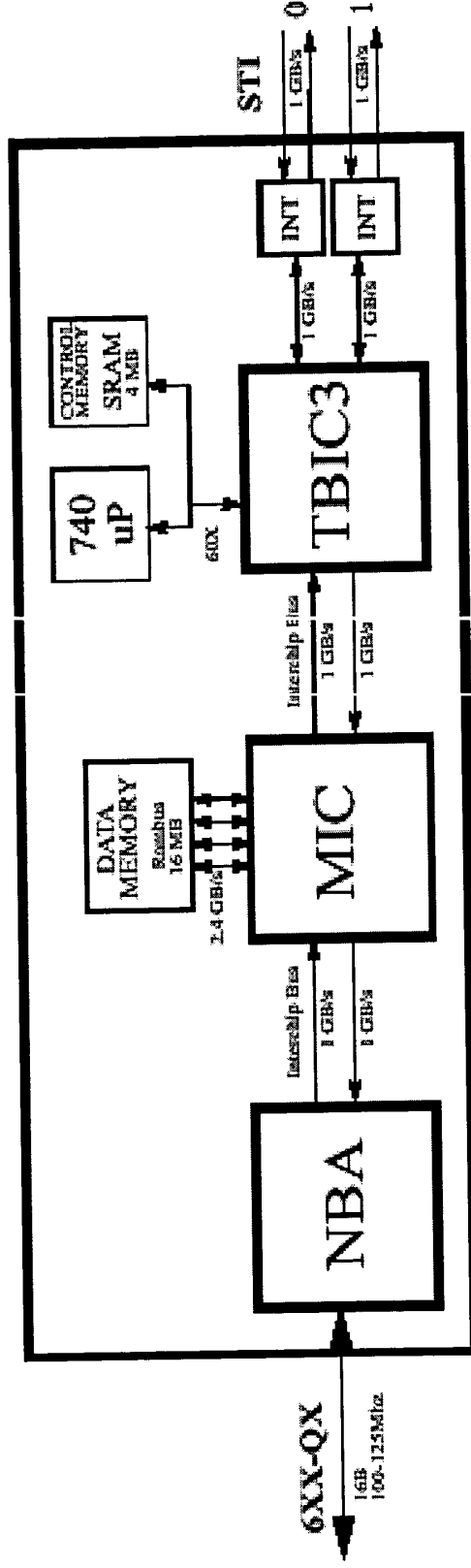
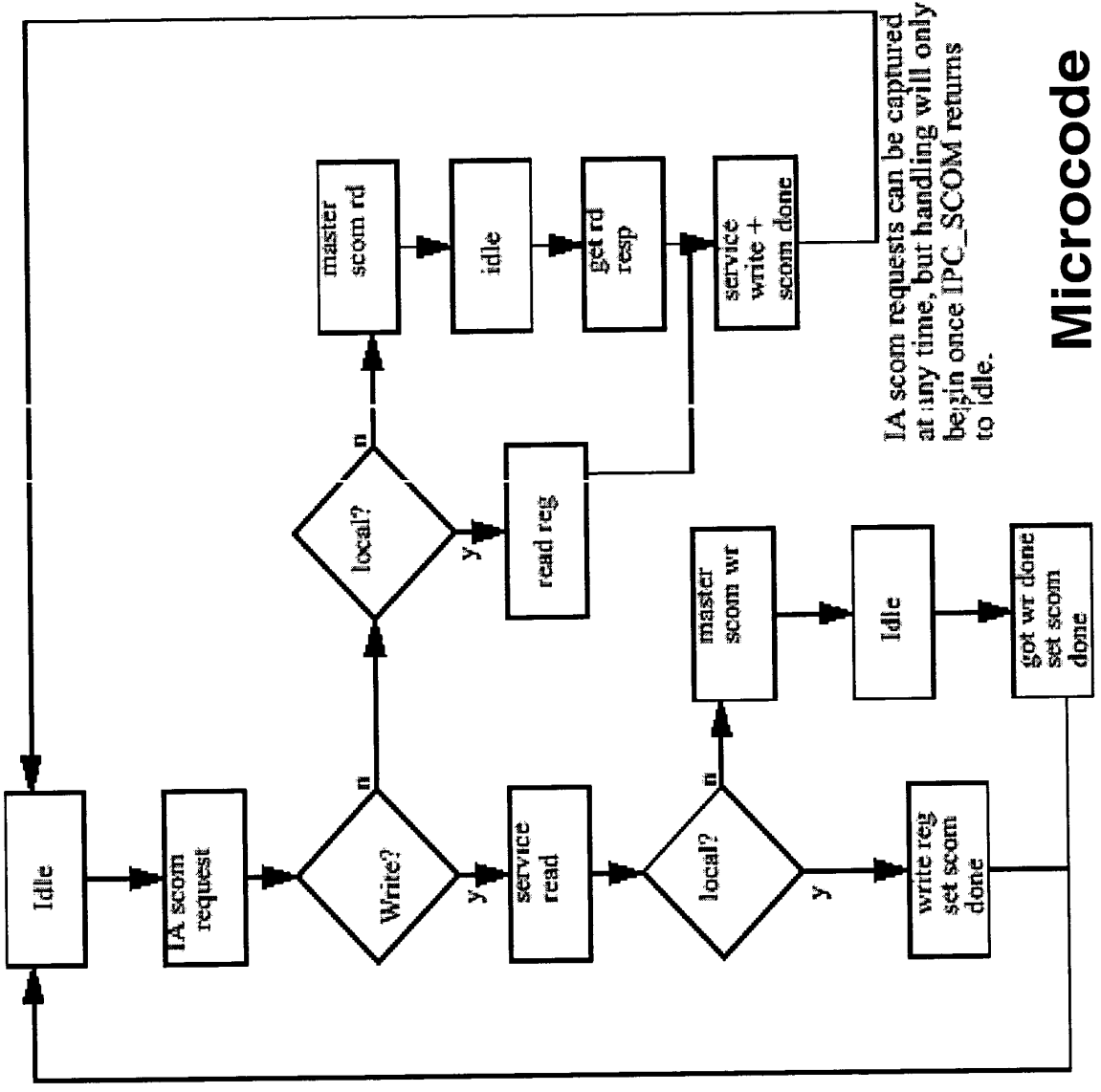


FIGURE 10. Colony Adapter

From page 32 of the spec – inclusion speculative

Figure 41

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Microcode

Figure 42

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AUTO TRACKING OF BAD PATHS

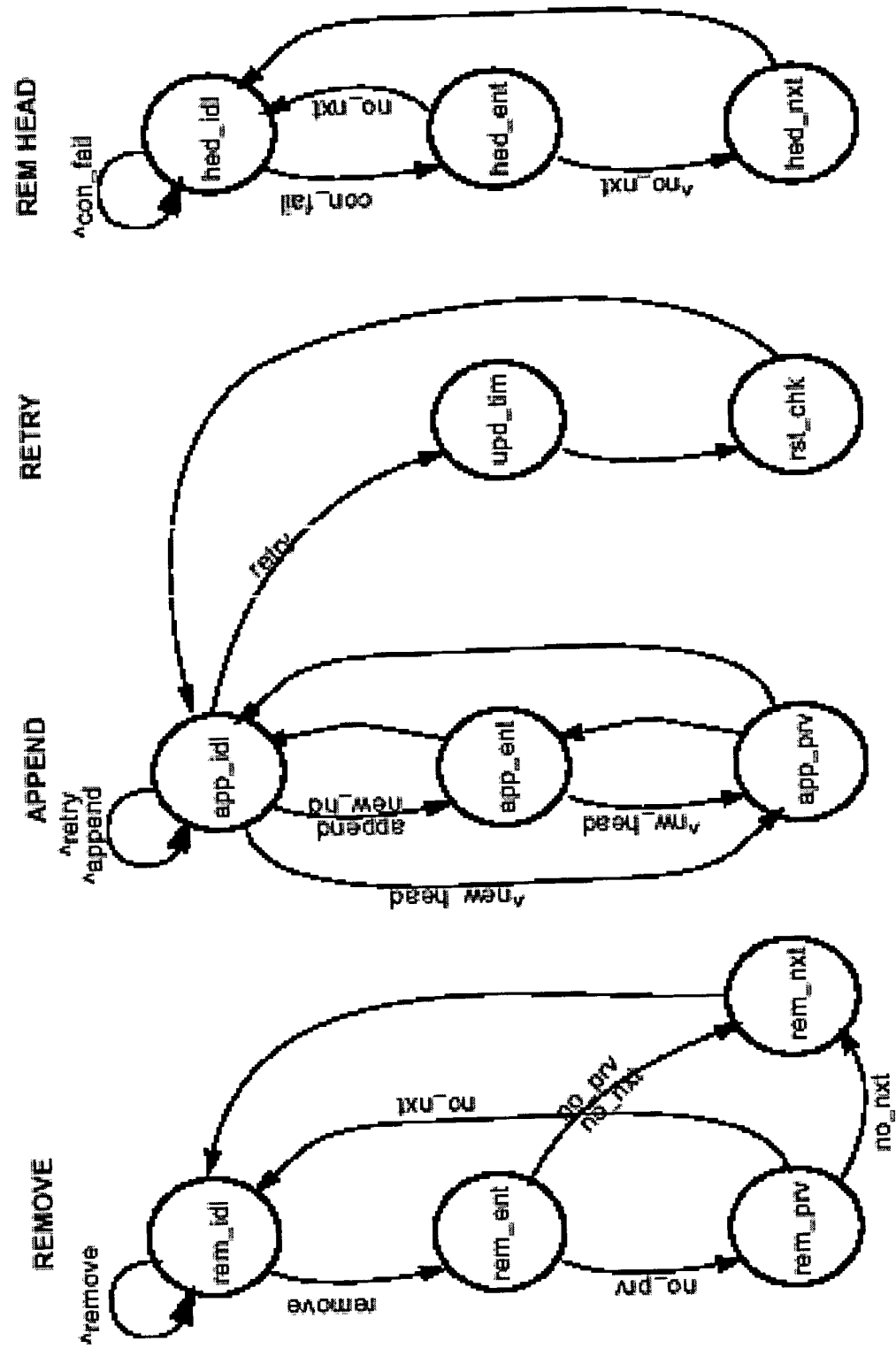


Figure 43

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Formatter

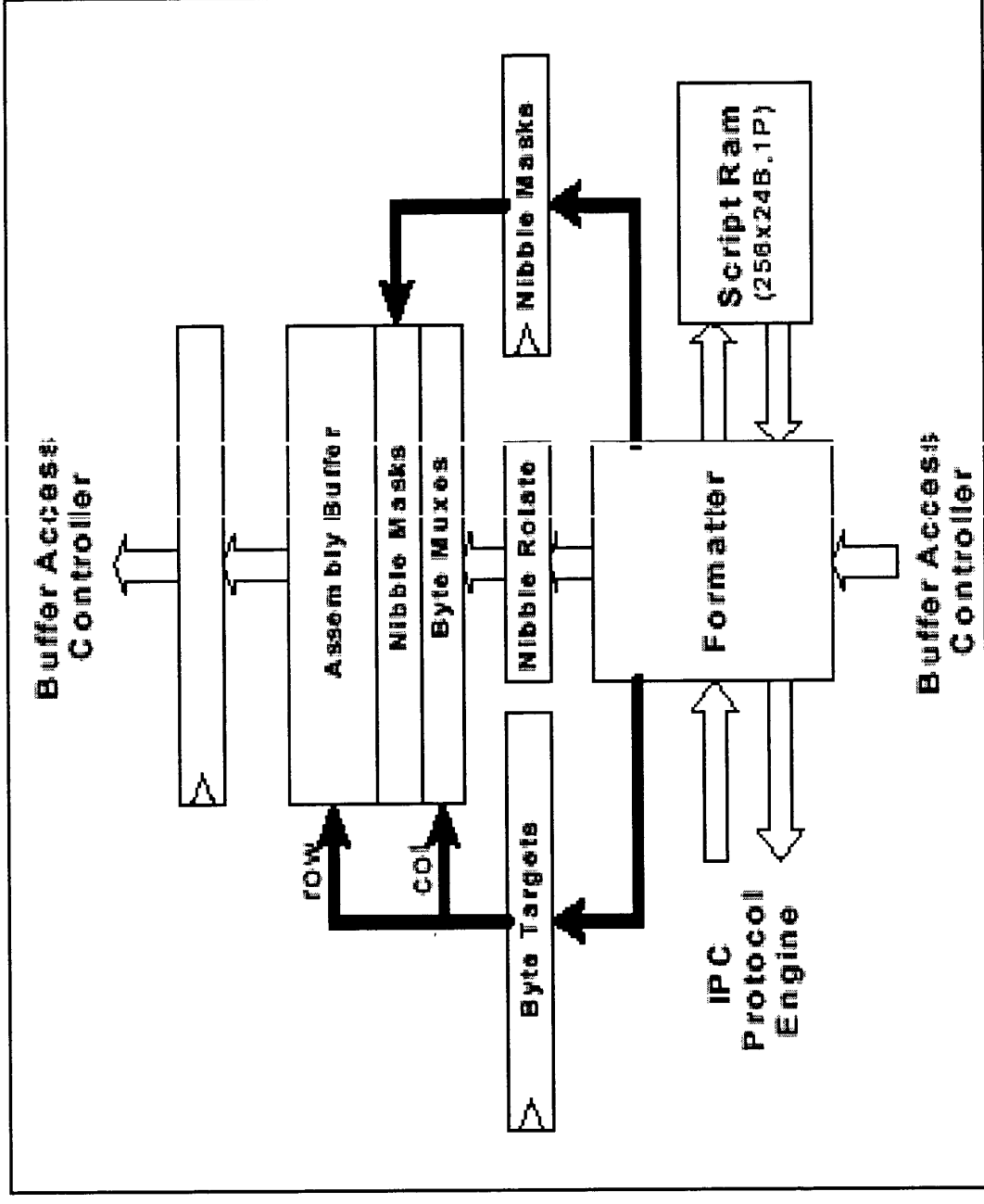
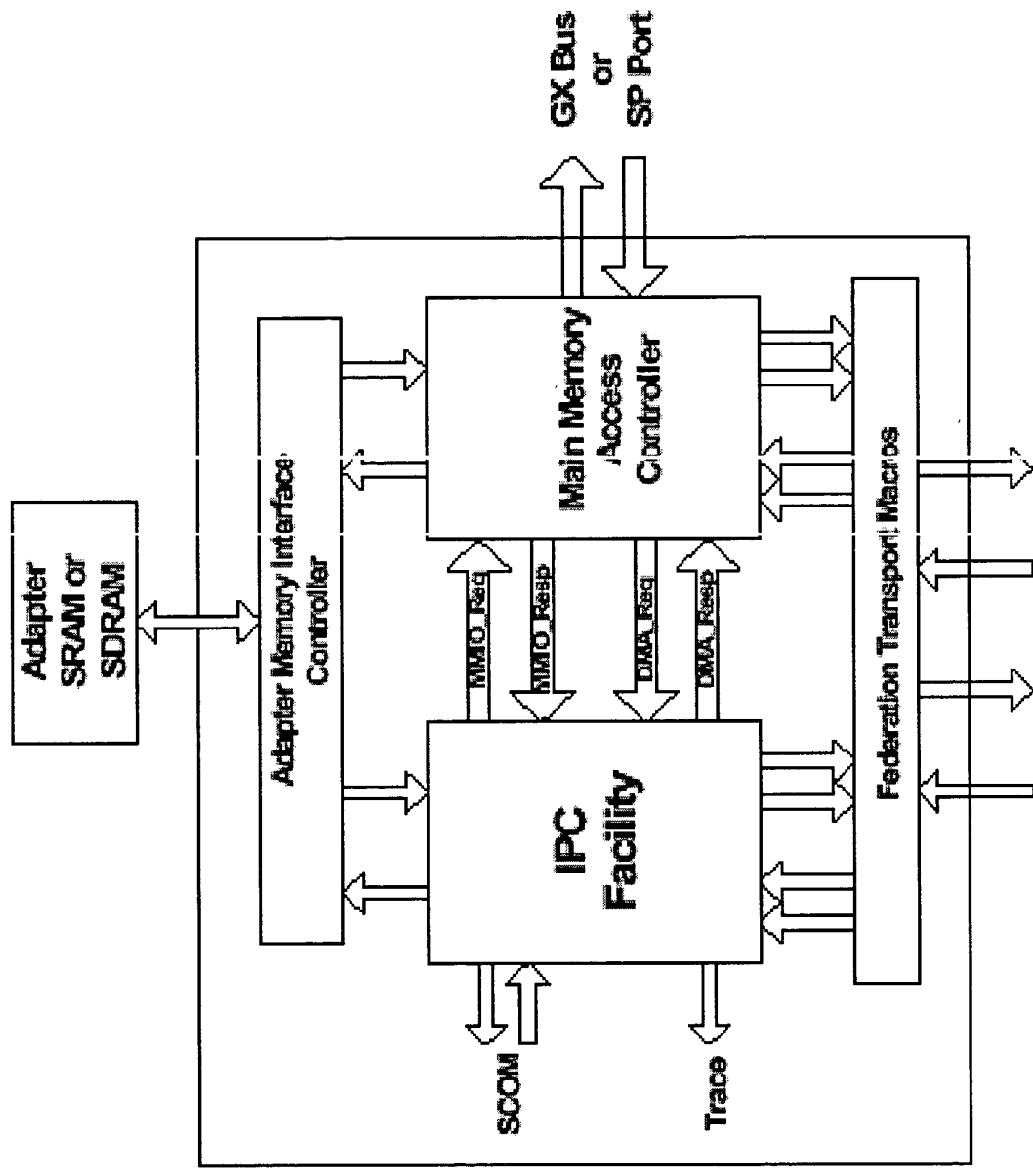


Figure 44

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Federation Fabric

Figure 45

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Section 18

- Legend**
- Extended external
 - Normal segment memory
 - ▨ Normal segment memory
 - Extended segment memory

Control Ring
(MIMO load)

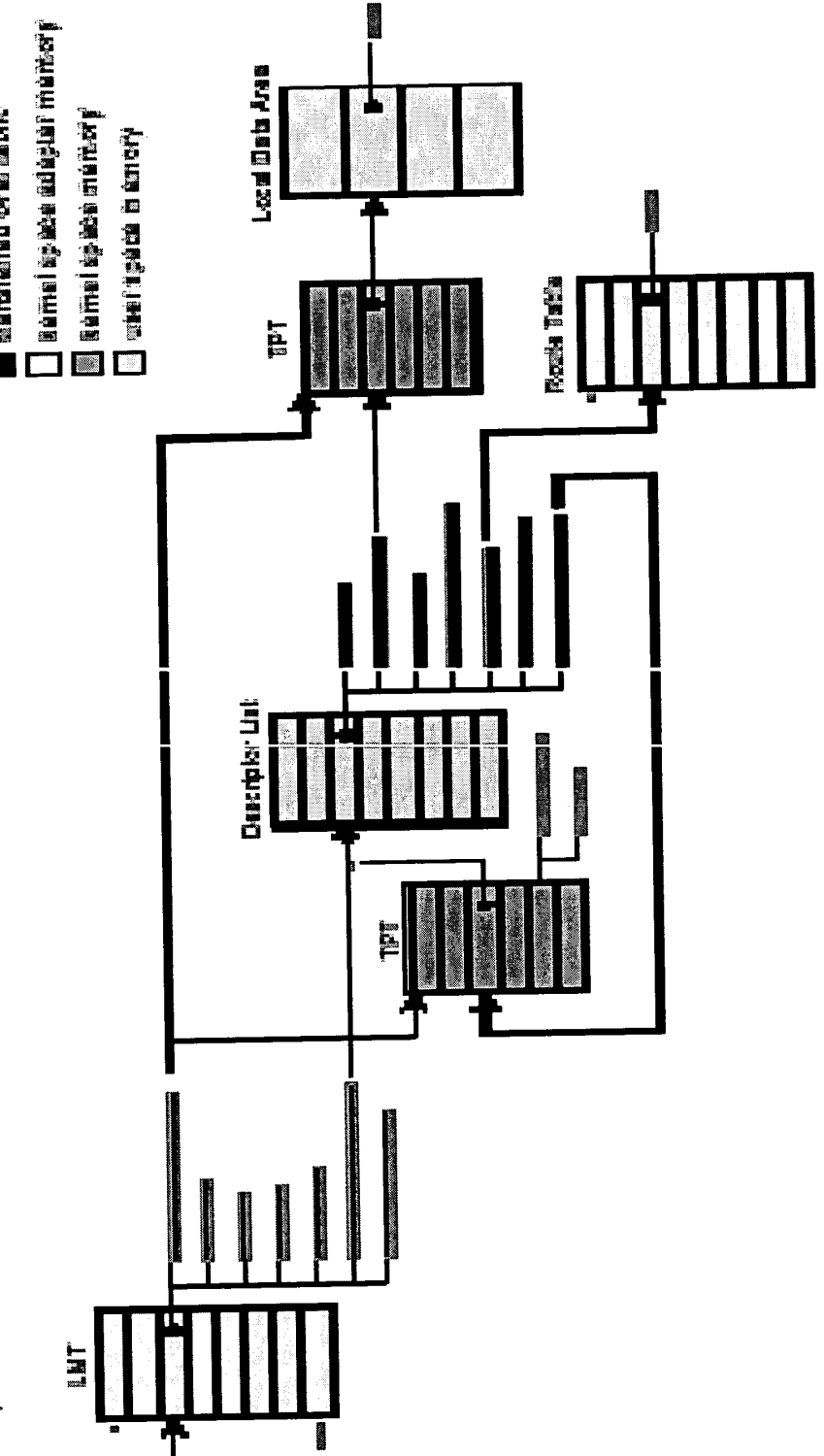


Figure 46

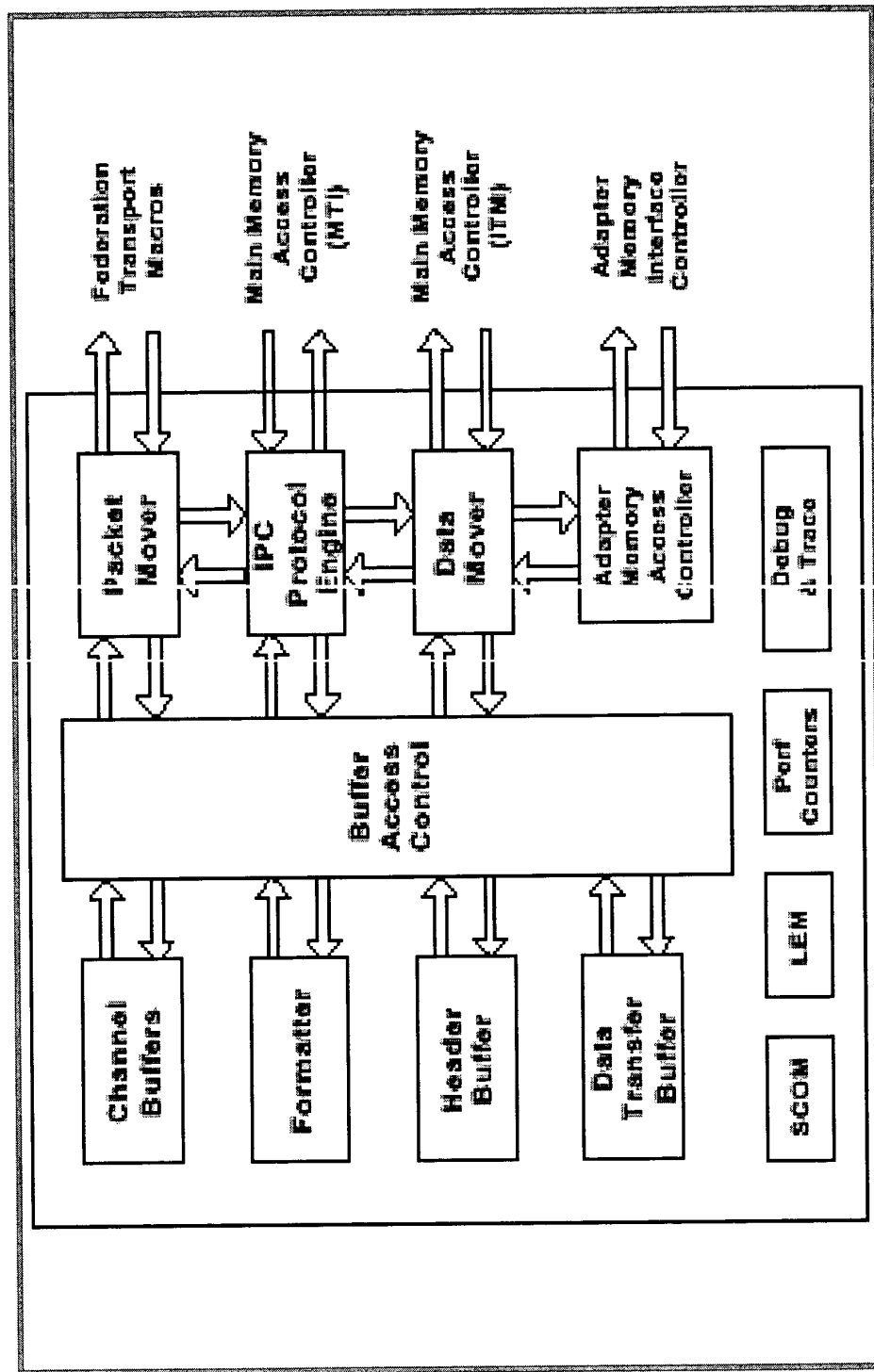


Figure 47

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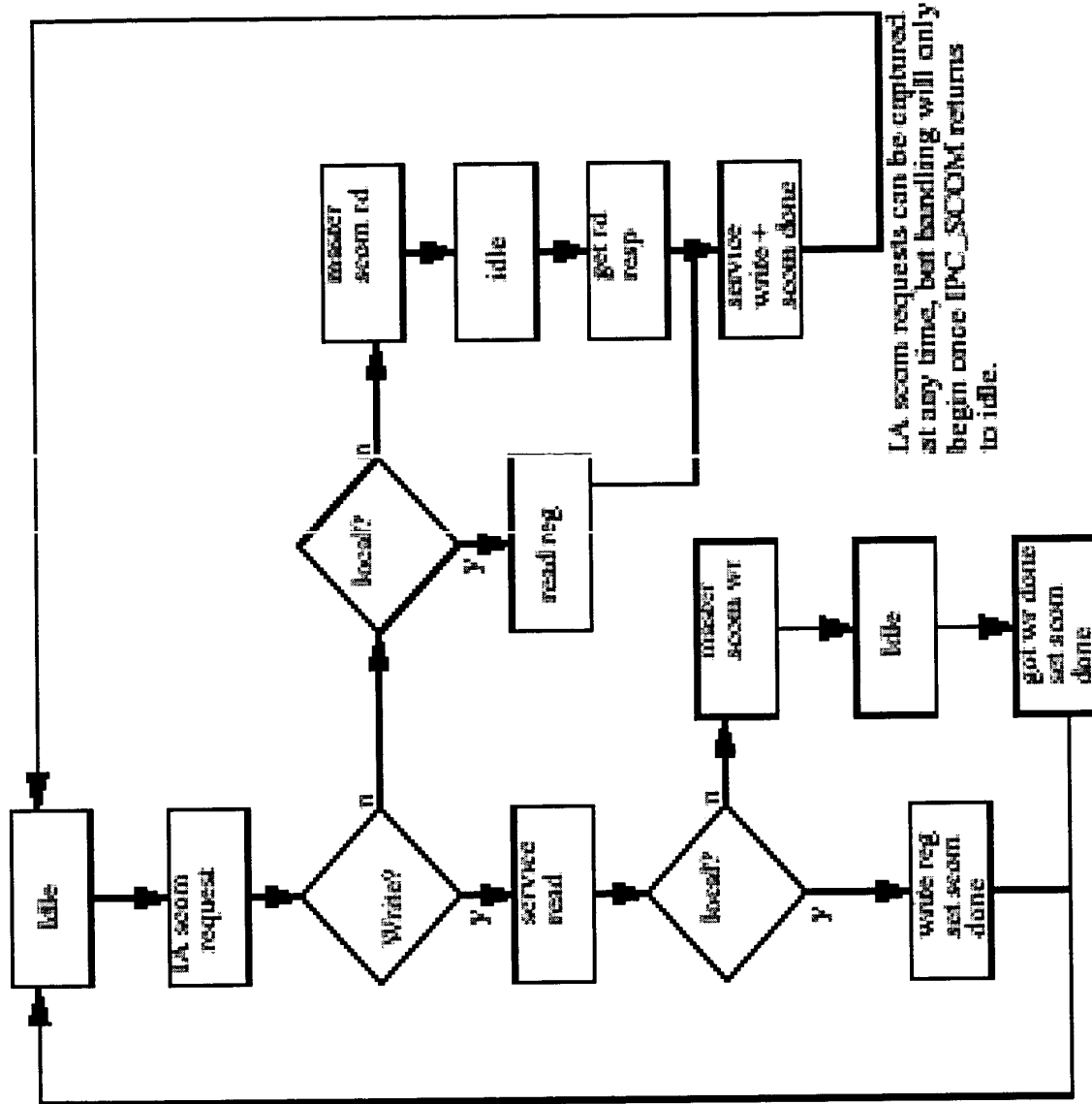


Figure 48

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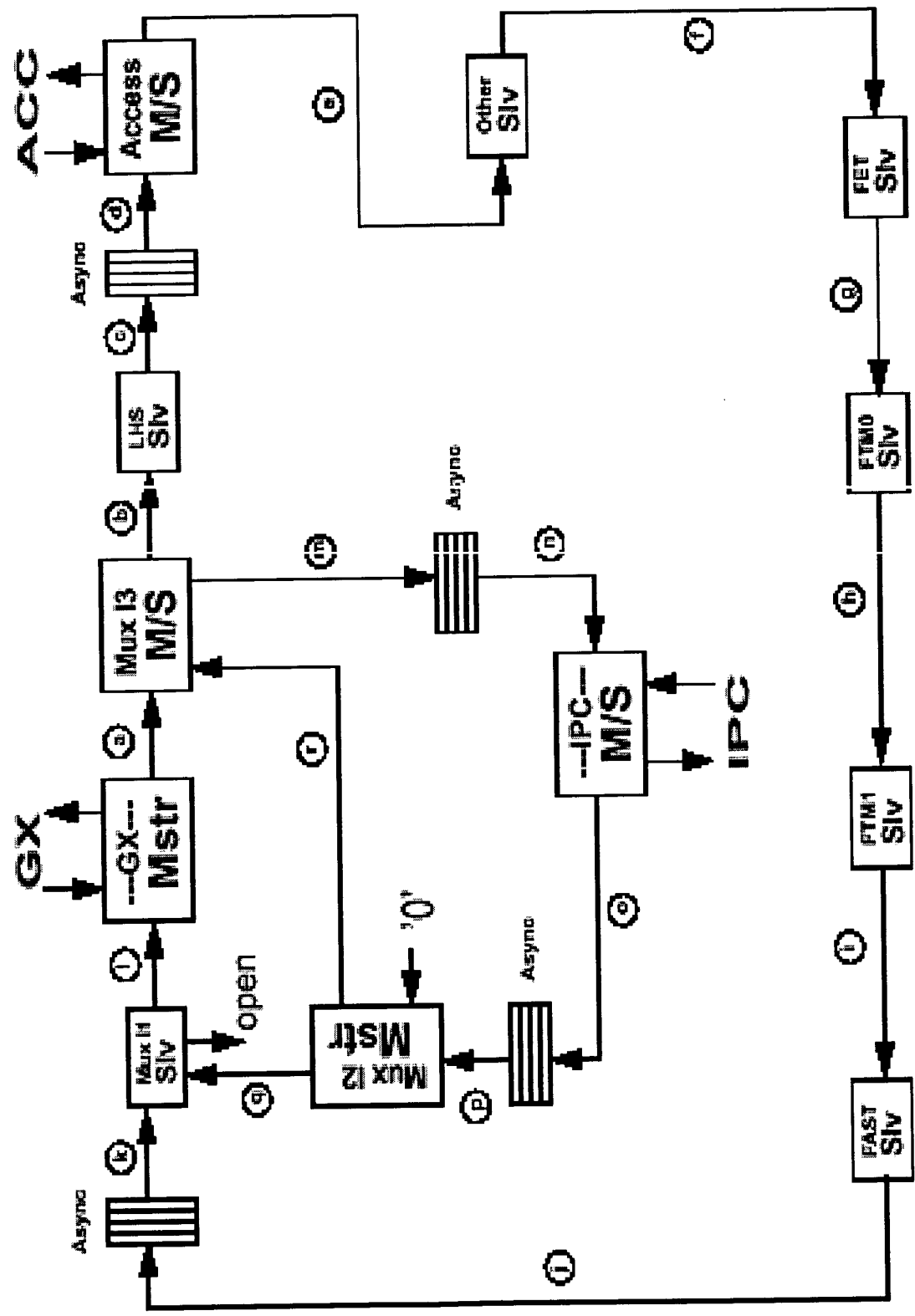


Figure 49

IPC Protocol Engine

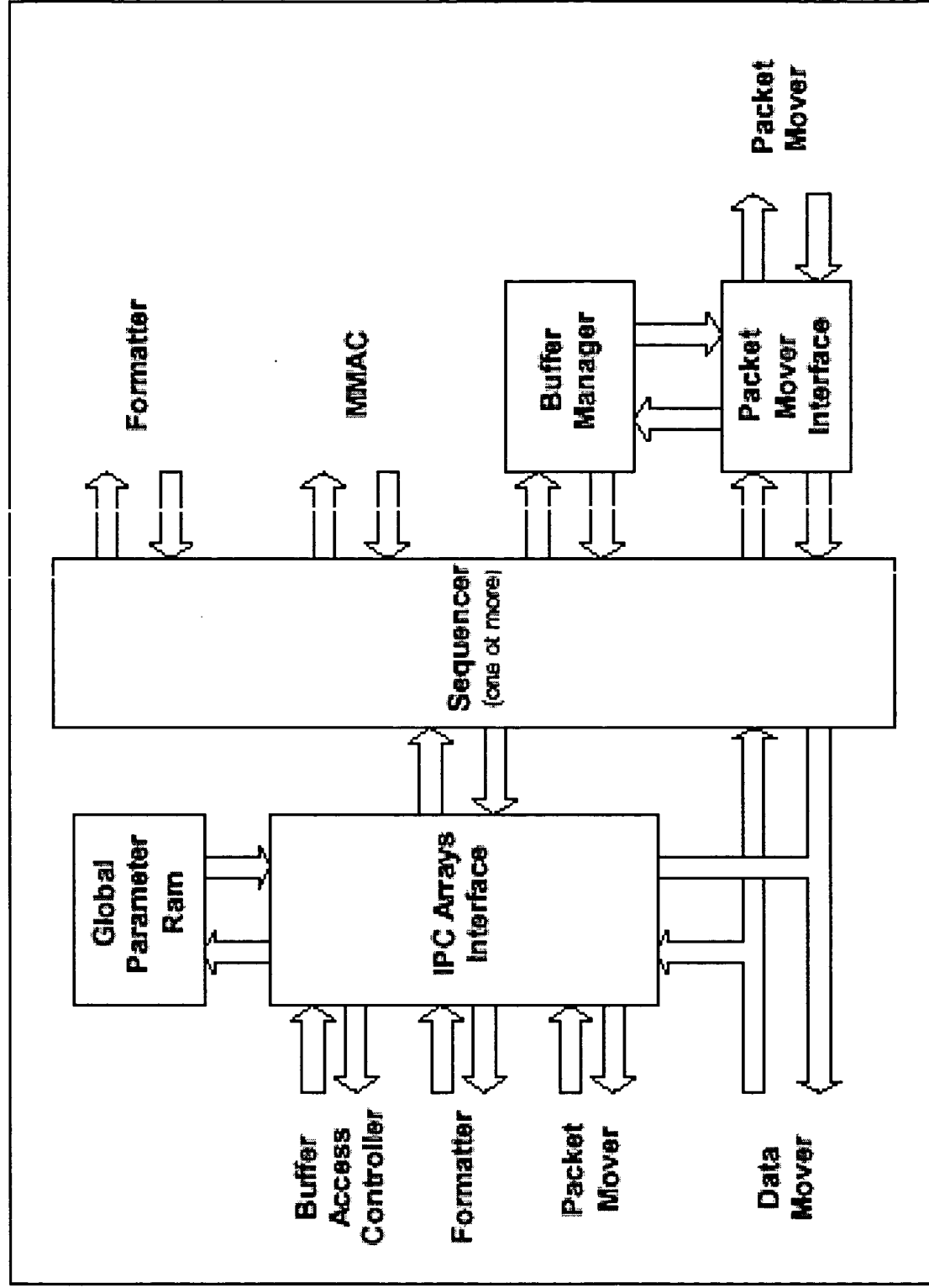


Figure 50